MAX II Architecture

Functional Description

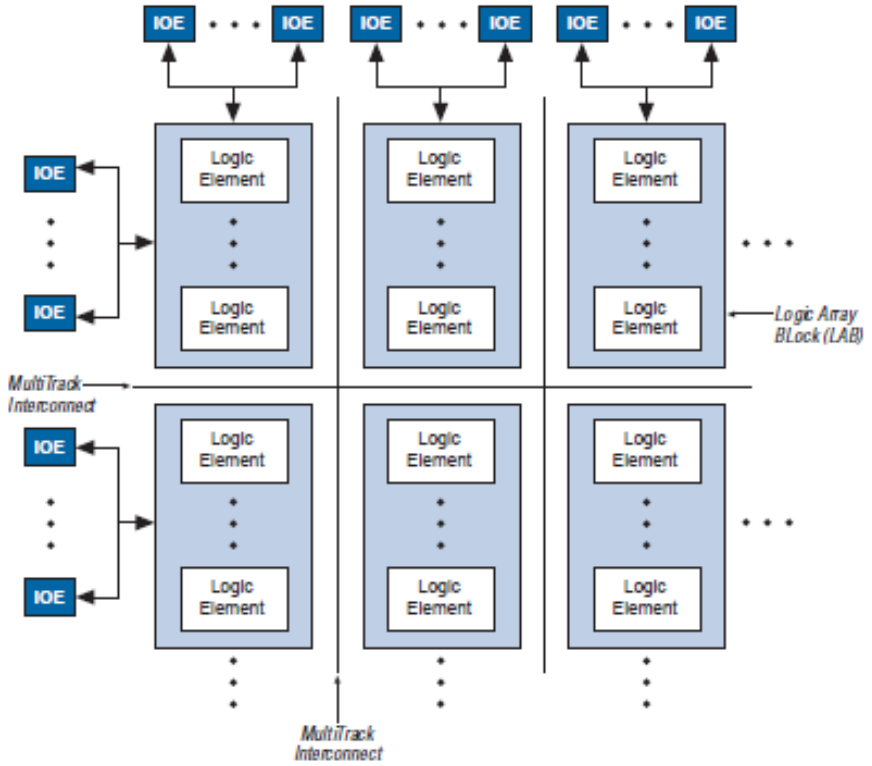
Functional block diagram

The logic array

MAX® II devices contain a two-dimensional row- and column-based architecture to implement custom logic. Row and column interconnects provide signal interconnects

between the logic array blocks (LABs).

Figure 2–1. MAX II Device Block Diagram



Each LAB consists of 10 LEs

LAB's

The logic array consists of LABs, with 10 logic elements (LEs) in each LAB. An LE is a small unit of logic providing efficient implementation of user logic functions.

LABs are grouped into rows and columns across the device

Figure 2–3. MAX II LAB Structure

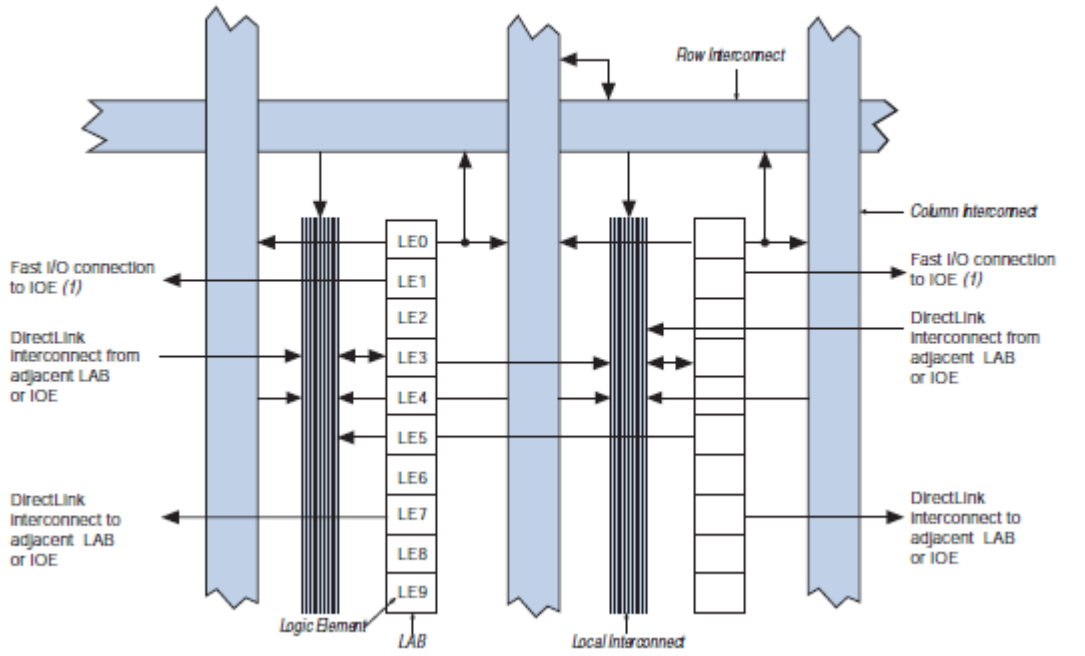
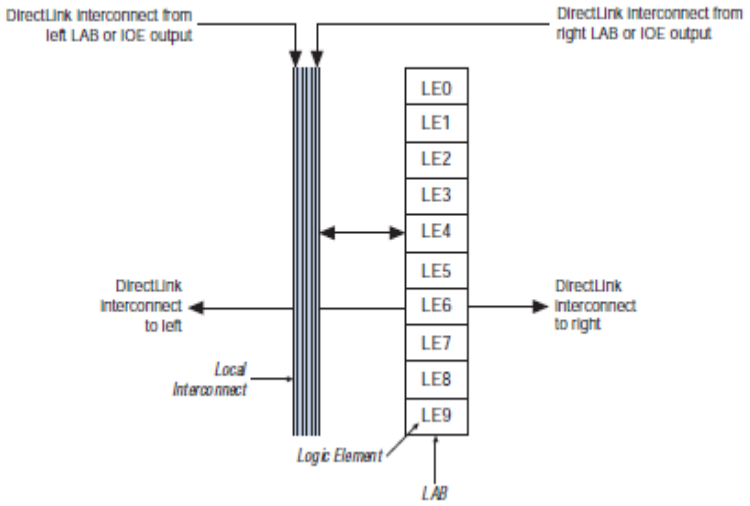


Figure 2–4. DirectLink Connection

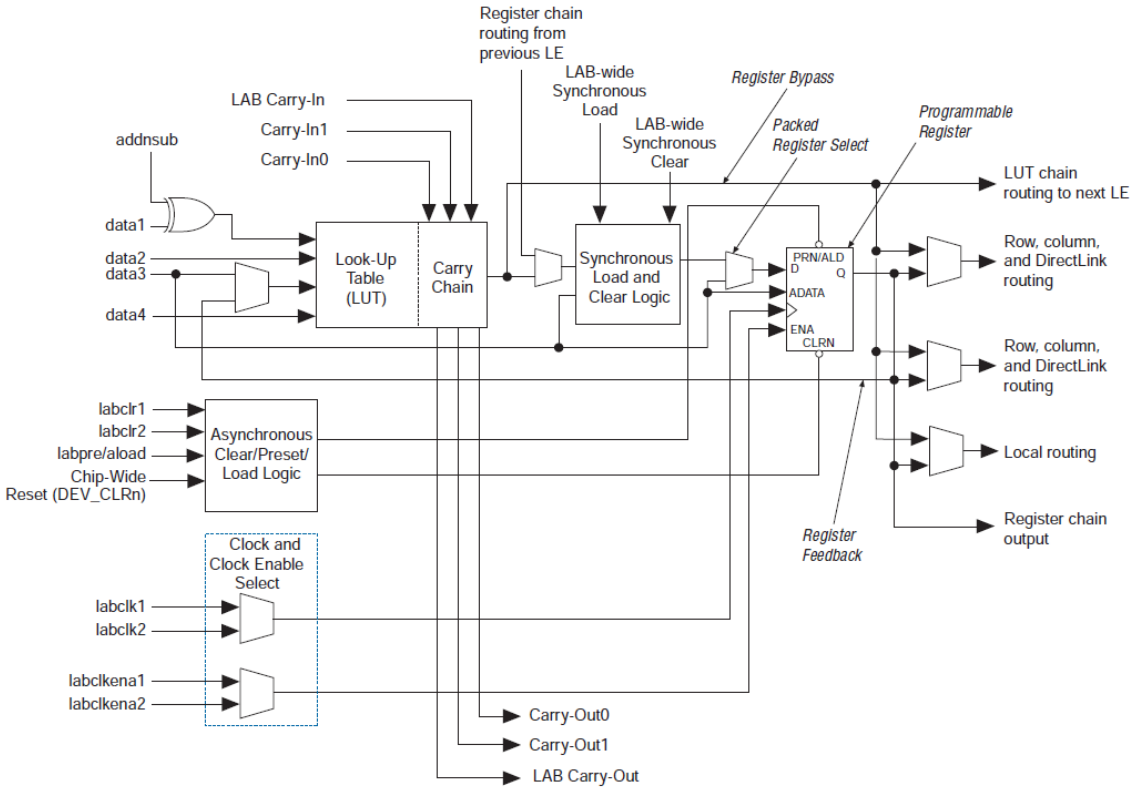


LAB Interconnects

The MultiTrack interconnect provides fast granular timing delays between LABs.

The fast routing between Les provides minimum timing delay for added levels of logic versus globally routed interconnect structures.

Figure 2–6. MAX II LE

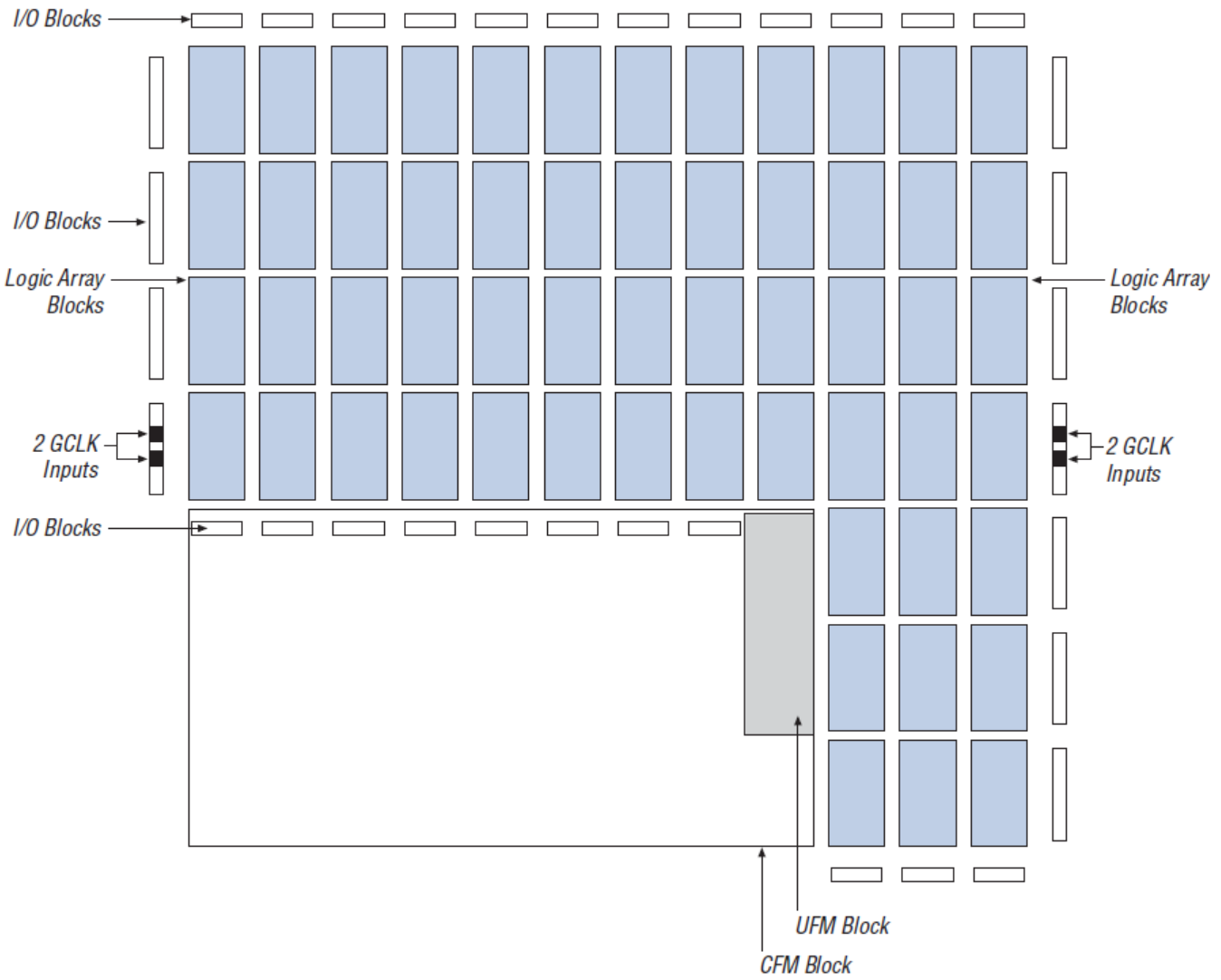


Logic Elements

The smallest unit of logic in the MAX II architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can implement any function of four variables.

Floorplan of a MAX II device

Figure 2–2. MAX II Device Floorplan *(Note 1)*



I/O Blocks

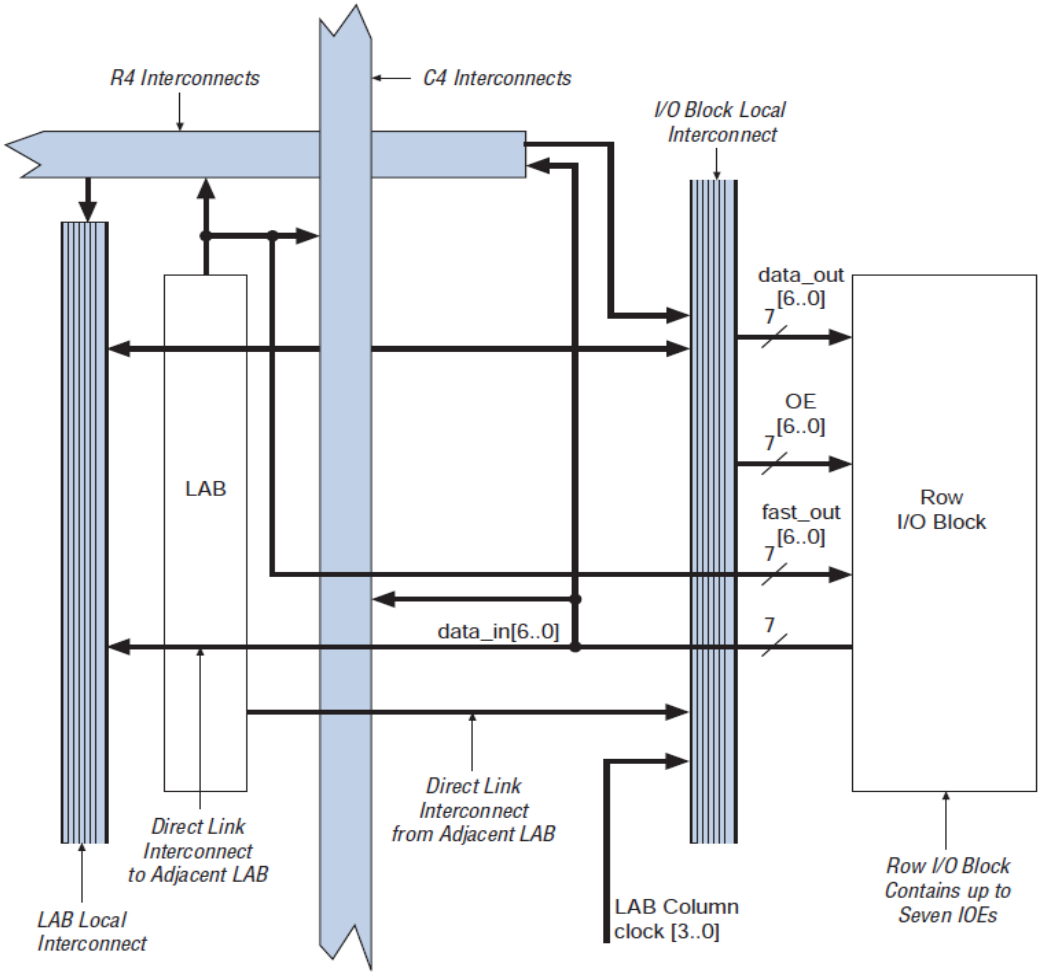
The IOEs are located in I/O blocks around the periphery of the MAX II device.

There are up to seven IOEs per row I/O block (5 maximum in the EPM240 device) and up to four IOEs per column I/O block.

Each column or row I/O block interfaces with its adjacent LAB and MultiTrack nterconnect to distribute signals throughout the device.

The row I/O blocks drive row, column, or DirectLink interconnects.

Figure 2–20. Row I/O Block Connection to the Interconnect *(Note 1)*



Column I/O block

The column I/O blocks drive column interconnects.

Figure 2–21. Column I/O Block Connection to the Interconnect *(Note 1)*

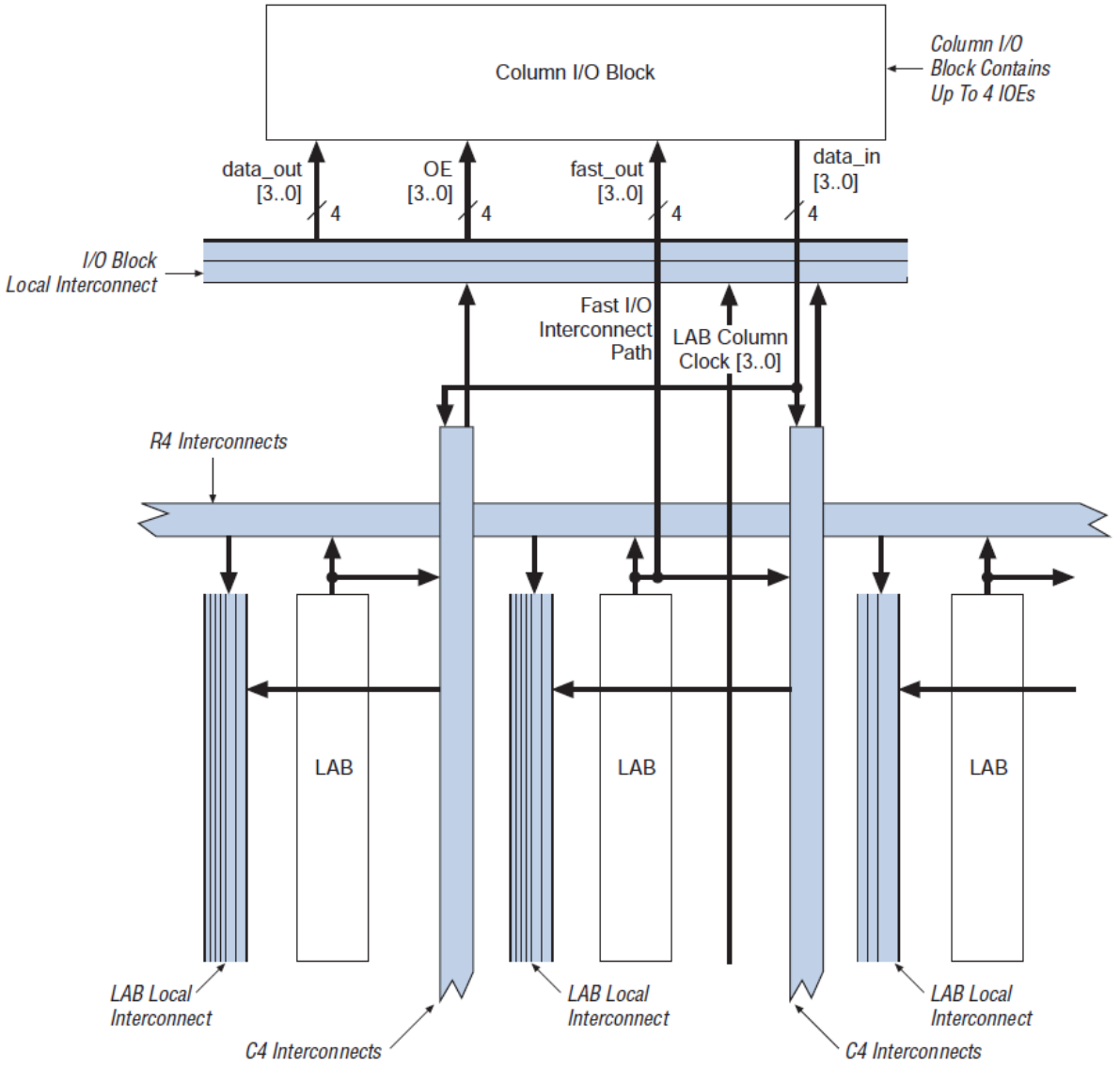
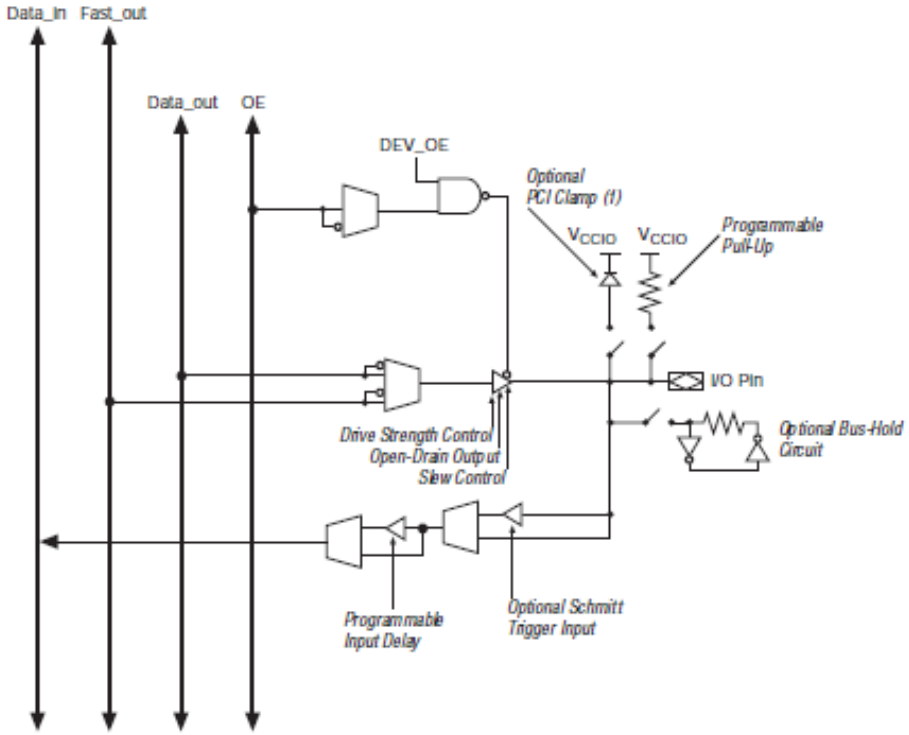


Figure 2–19. MAX II IOE Structure



The MAX II device I/O pins are fed by I/O elements (IOE) located at the ends of LAB
rows and columns around the periphery of the device. Each IOE contains a bidirectional I/O buffer with several advanced features. I/O pins support Schmitt
trigger inputs and various single-ended standards, such as 66-MHz, 32-bit PCI, and
LVTTL.