

Pin oversigt til DE1 board fra Altera

Push Button Switch Pin List

Table 2–10 lists the FPGA pins assigned to the push button switches.

<i>Table 2–10. Push Button Switch FPGA Pin Connections</i>		
Switch	FPGA Pin	Description
KEY[0]	PIN_R22	Pushbutton[0]
KEY[1]	PIN_R21	Pushbutton[1]
KEY[2]	PIN_T22	Pushbutton[2]
KEY[3]	PIN_T21	Pushbutton[3]

Toggle Switch Pin List

Table 2–11 lists the FPGA pins assigned to the toggle switches.

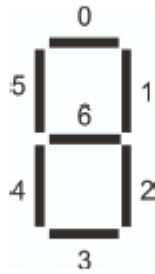
<i>Table 2–11. Toggle Switch FPGA Pin Connections</i>		
Switch	FPGA Pin	Description
SW[0]	PIN_L22	Toggle Switch[0]
SW[1]	PIN_L21	Toggle Switch[1]
SW[2]	PIN_M22	Toggle Switch[2]
SW[3]	PIN_V12	Toggle Switch[3]
SW[4]	PIN_W12	Toggle Switch[4]
SW[5]	PIN_U12	Toggle Switch[5]
SW[6]	PIN_U11	Toggle Switch[6]
SW[7]	PIN_M2	Toggle Switch[7]
SW[8]	PIN_M1	Toggle Switch[8]
SW[9]	PIN_L2	Toggle Switch[9]

LED Pin List

Table 2–12 lists the FPGA pins assigned to the LEDs.

Signal Name	FPGA Pin	Description
LEDR[0]	PIN_R20	LED Red[0]
LEDR[1]	PIN_R19	LED Red[1]
LEDR[2]	PIN_U19	LED Red[2]
LEDR[3]	PIN_Y19	LED Red[3]
LEDR[4]	PIN_T18	LED Red[4]
LEDR[5]	PIN_V19	LED Red[5]
LEDR[6]	PIN_Y18	LED Red[6]
LEDR[7]	PIN_U18	LED Red[7]
LEDR[8]	PIN_R18	LED Red[8]
LEDR[9]	PIN_R17	LED Red[9]
LEDG[0]	PIN_U22	LED Green[0]
LEDG[1]	PIN_U21	LED Green[1]
LEDG[2]	PIN_V22	LED Green[2]
LEDG[3]	PIN_V21	LED Green[3]
LEDG[4]	PIN_W22	LED Green[4]
LEDG[5]	PIN_W21	LED Green[5]
LEDG[6]	PIN_Y22	LED Green[6]
LEDG[7]	PIN_Y21	LED Green[7]

Figure 2–17. Segment Index and Position



Seven-Segment Display Pin List

Table 2–13 lists the FPGA pins assigned to the display segments.

Signal Name	FPGA Pin	Description
HEX0[0]	PIN_J2	Seven-Segment segment 0[0]
HEX0[1]	PIN_J1	Seven-Segment segment 0[1]
HEX0[2]	PIN_H2	Seven-Segment segment 0[2]
HEX0[3]	PIN_H1	Seven-Segment segment 0[3]
HEX0[4]	PIN_F2	Seven-Segment segment 0[4]
HEX0[5]	PIN_F1	Seven-Segment segment 0[5]
HEX0[6]	PIN_E2	Seven-Segment segment 0[6]
HEX1[0]	PIN_E1	Seven-Segment segment 1[0]
HEX1[1]	PIN_H6	Seven-Segment segment 1[1]

Table 2–13. Seven-Segment Display FPGA Pin Connections (Part 2 of 2)

Signal Name	FPGA Pin	Description
HEX1[2]	PIN_H5	Seven-Segment segment 1[2]
HEX1[3]	PIN_H4	Seven-Segment segment 1[3]
HEX1[4]	PIN_G3	Seven-Segment segment 1[4]
HEX1[5]	PIN_D2	Seven-Segment segment 1[5]
HEX1[6]	PIN_D1	Seven-Segment segment 1[6]
HEX2[0]	PIN_G5	Seven-Segment segment 2[0]
HEX2[1]	PIN_G6	Seven-Segment segment 2[1]
HEX2[2]	PIN_C2	Seven-Segment segment 2[2]
HEX2[3]	PIN_C1	Seven-Segment segment 2[3]
HEX2[4]	PIN_E3	Seven-Segment segment 2[4]
HEX2[5]	PIN_E4	Seven-Segment segment 2[5]
HEX2[6]	PIN_D3	Seven-Segment segment 2[6]
HEX3[0]	PIN_F4	Seven-Segment segment 3[0]
HEX3[1]	PIN_D5	Seven-Segment segment 3[1]
HEX3[2]	PIN_D6	Seven-Segment segment 3[2]
HEX3[3]	PIN_J4	Seven-Segment segment 3[3]
HEX3[4]	PIN_L8	Seven-Segment segment 3[4]
HEX3[5]	PIN_F3	Seven-Segment segment 3[5]
HEX3[6]	PIN_D4	Seven-Segment segment 3[6]

Expansion Header Pin List

Table 2–14 lists the FPGA pins assigned to the expansion headers.

Table 2–14. Expansion Header FPGA Pin Connections (Part 1 of 3)

Signal Name	FPGA Pin	Description
GPIO_0[0]	PIN_A13	GPIO Connection 0[0]
GPIO_0[1]	PIN_B13	GPIO Connection 0[1]
GPIO_0[2]	PIN_A14	GPIO Connection 0[2]
GPIO_0[3]	PIN_B14	GPIO Connection 0[3]