

Start af nyt VHDL projekt i Quartus II

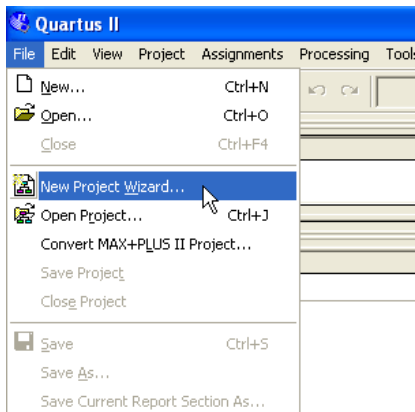
Det følgende er ikke fremstillet som en brugsanvisning der gennemgår alle de muligheder der er omkring oprettelse af et VHDL projekt i Quartus II men kun som en enkelt måde at komme i gang på. Dokumentet udleveres som en Word file til eleven således at han/hun selv kan fremstille en mere fuldstændig brugsanvisning som en del af sit portofolio.

VHDL betyder: *Very high speed integrated circuit Hardware Description Language*

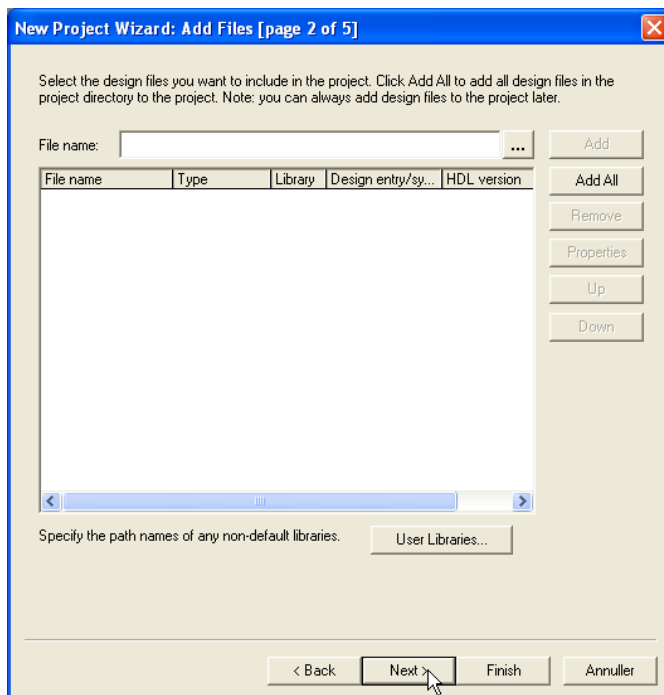
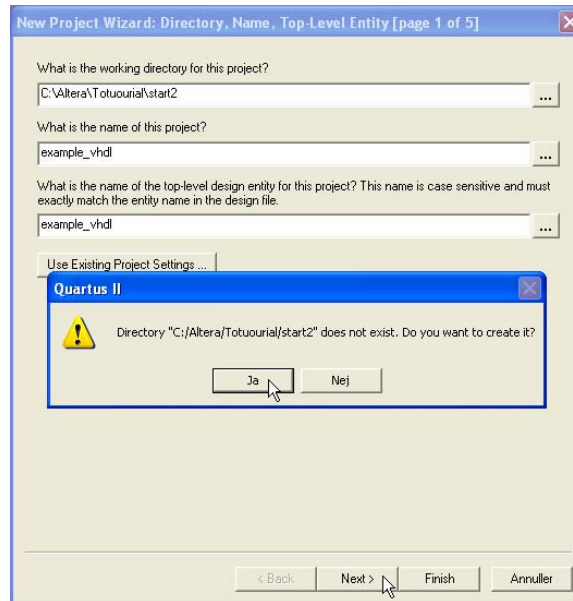
Udførelsen forudsætter at ” *Start af nyt schematic projekt i Quartus II*” er udført da dele derfra skal gentages i denne øvelse, ligesom denne øvelse stort set er uden tekst og forklaringer.

Ole Rasmussen 2010

Start med "New Project Wizard"



Og opret en mappe med navnet start2 under
C:\Altera\Totuourial
Og giv projektet navnet: **example_vhdl**



Vælg family: CycloneII og Target device til Auto

New Project Wizard: Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.

Device family
Family: **Cyclone II**
Devices: **All**

Show in 'Available device' list
Package: **Any**
Pin count: **Any**
Speed grade: **Any**

Target device
 Auto device selected by the Filter
 Specific device selected in 'Available devices' list

Available devices:

Name	Core v...	LEs	User I/...	Memor...	Embed...	PLL
EP2C5AF256A7	1.2V	4608	158	119808	26	2
EP2C5AF256B8	1.2V	4608	158	119808	26	2
EP2C5AT144A7	1.2V	4608	89	119808	26	2
EP2C5F256C6	1.2V	4608	158	119808	26	2
EP2C5F256C7	1.2V	4608	158	119808	26	2
EP2C5F256C8	1.2V	4608	158	119808	26	2
EP2C5F256B8	1.2V	4608	158	119808	26	2
EP2C5Q208C7	1.2V	4608	142	119808	26	2
EP2C5Q208C7	1.2V	4608	142	119808	26	2

Companion device:
HardCopy: **None**
 Limit DSP & RAM to HardCopy device resources

< Back **Next >** Finish Annuller

New Project Wizard: EDA Tool Settings [page 4 of 5]

Specify the other EDA tools -- in addition to the Quartus II software -- used with the project.

Design Entry/Synthesis
Tool name: **<None>**
Format: **None**
 Run this tool automatically to synthesize the current design

Simulation
Tool name: **<None>**
Format: **None**
 Run gate-level simulation automatically after compilation

Timing Analysis
Tool name: **<None>**
Format: **None**
 Run this tool automatically after compilation

< Back **Next >** Finish Annuller

New Project Wizard: Summary [page 5 of 5]

When you click Finish, the project will be created with the following settings:

Project directory:
C:/Altera/Tutorial/start2/

Project name: example_vhdl
Top-level design entity: example_vhdl
Number of files added: 0
Number of user libraries added: 0

Device assignments:
Family name: Cyclone II
Device: AUTO

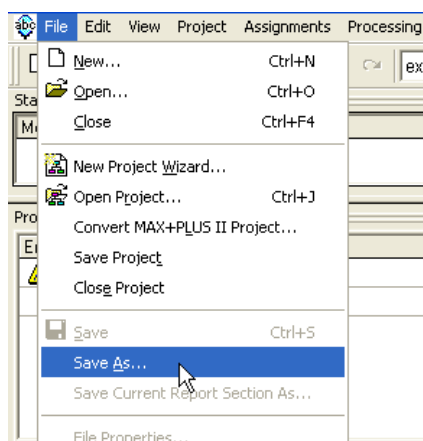
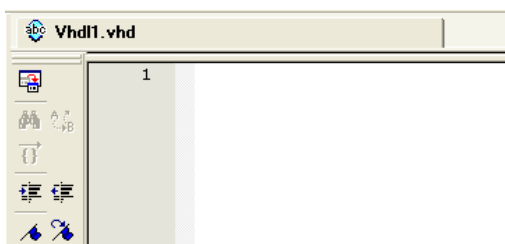
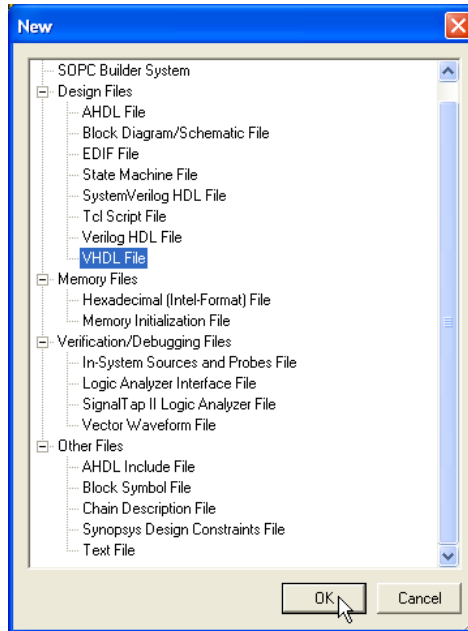
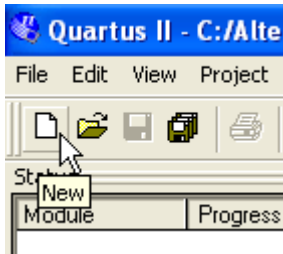
EDA tools:
Design entry/synthesis: <None>
Simulation: <None>
Timing analysis: <None>

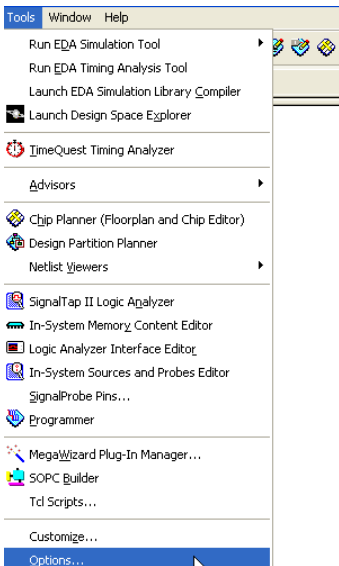
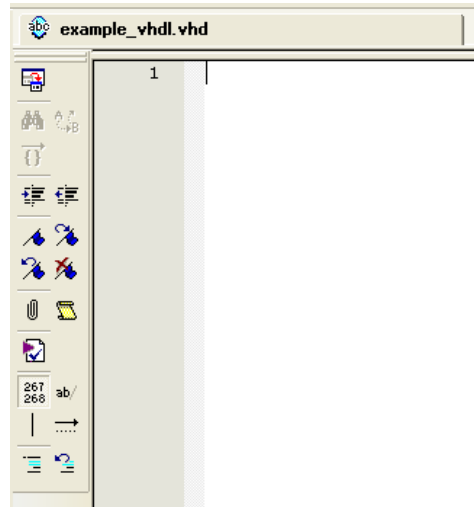
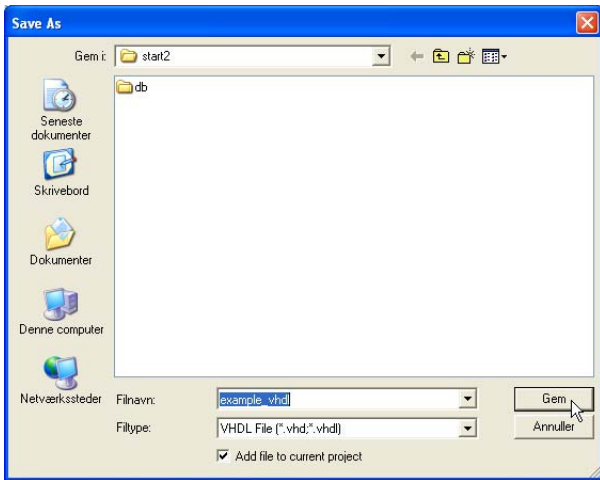
Operating conditions:
Core voltage: n/a
Junction temperature range: n/a

< Back Next > **Finish** Annuller

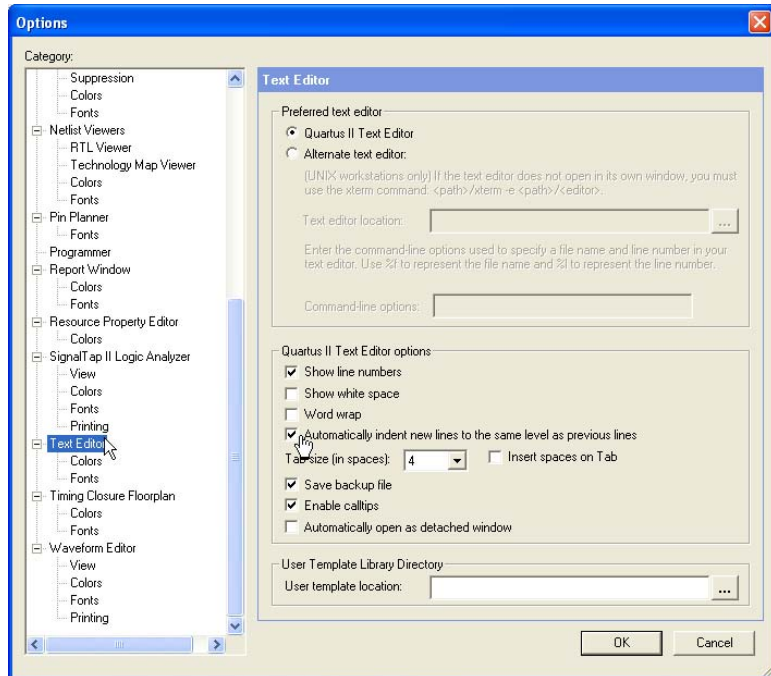
Du skal nu oprette en VHDL file.

(Very high speed integrated circuit Hardware Description Language)

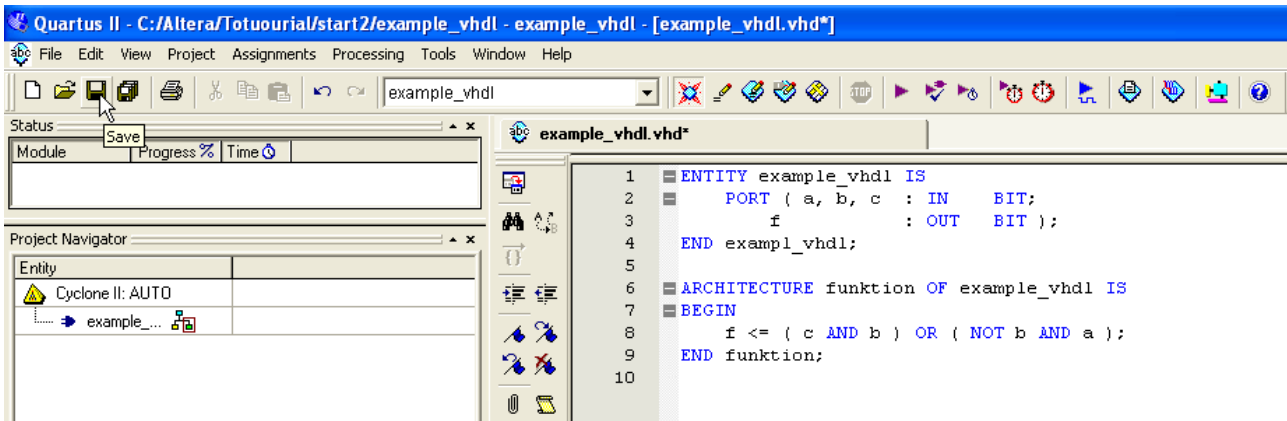




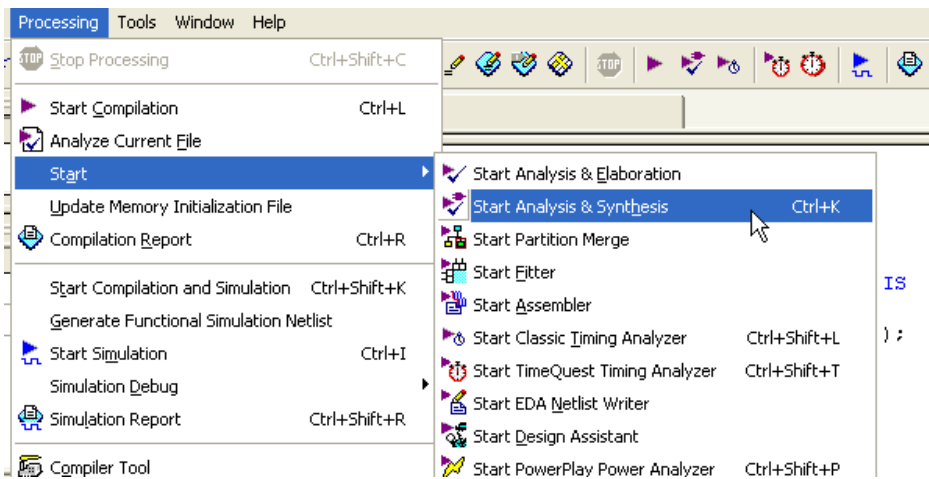
Når du skriver kildeteksten er det smart at der rykkes ind til ovenstående linje når du trykker <enter>.



Skriv kildeteksten som vist nedenfor.

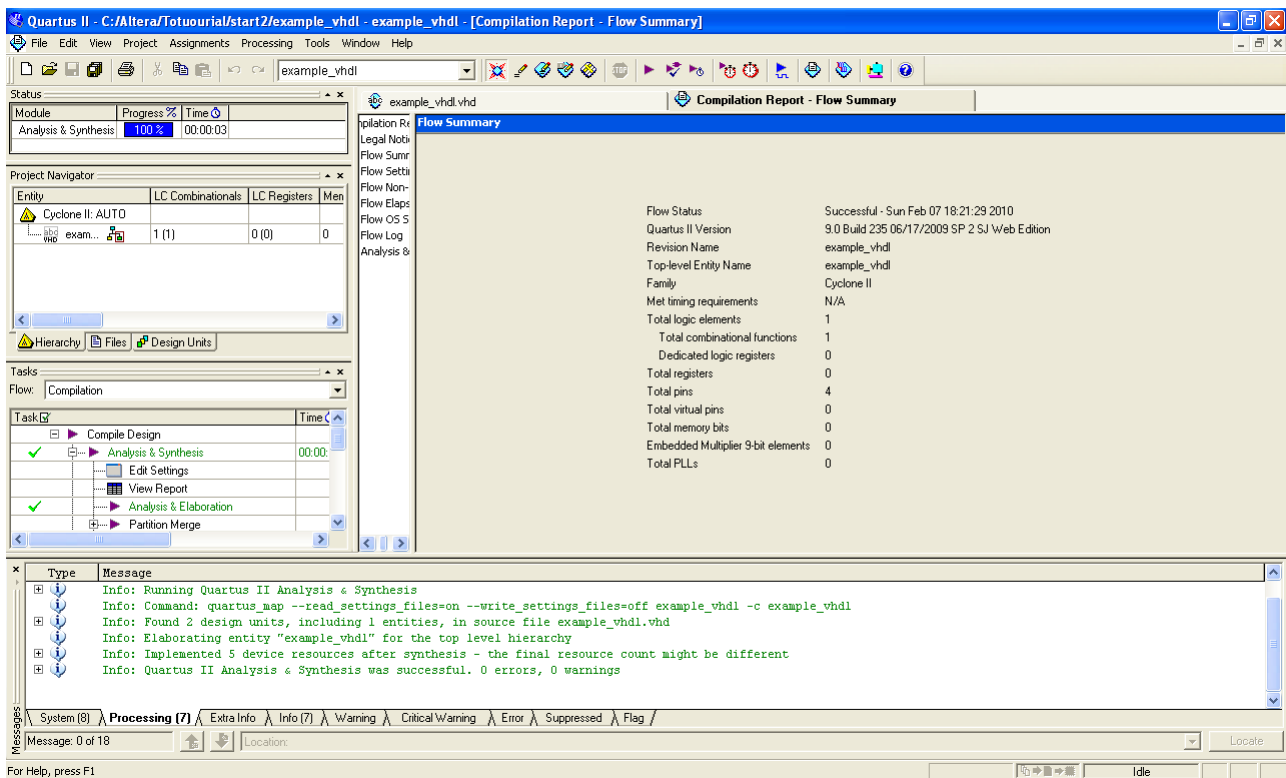


Denne gang kan du prøve at starte "Analysis & Synthesis" som vist nedenfor eller med <Ctrl+k>



Der fik du nok en del fejl. I det eksempel jeg har lavet er fejlen i linje 4.

Når alle fejl er rettet ser skærmen nok ud som nedenfor.



Prøv om du kan finde en mening med kildeteksten.

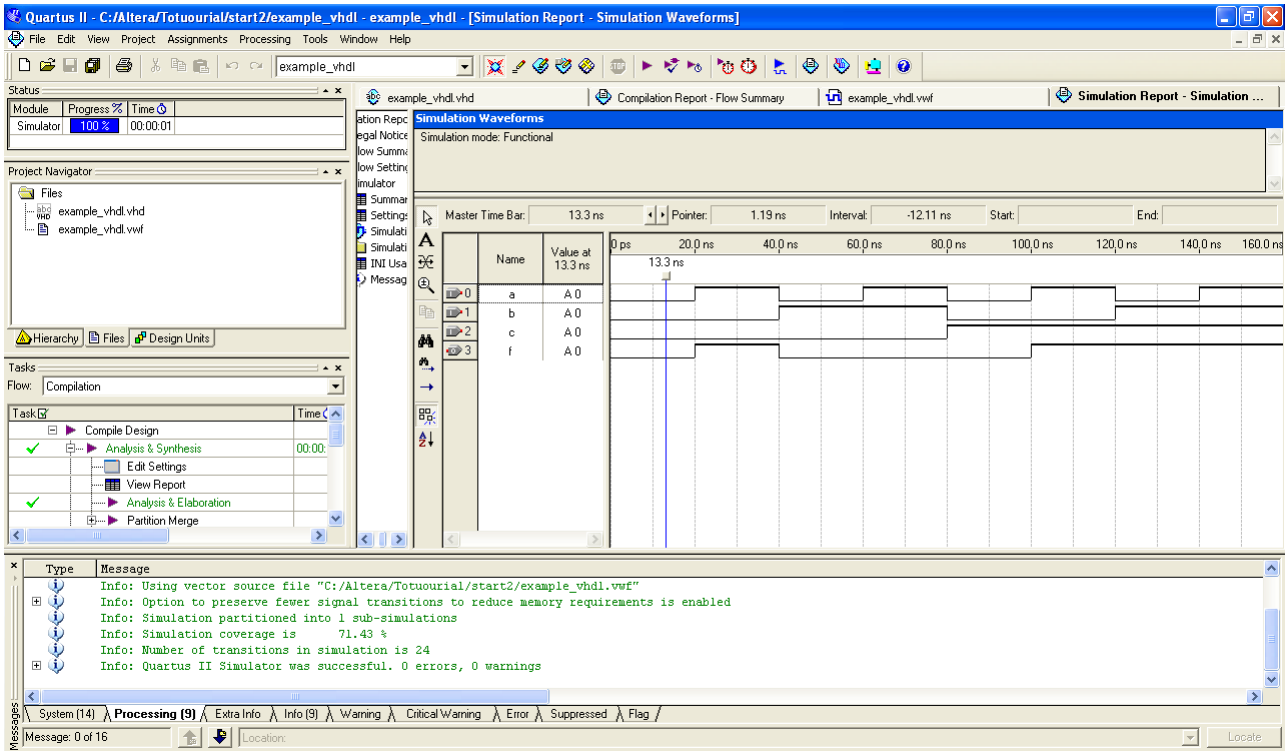
F.eks. hvorfor står noget med blå skrift?

```
ENTITY example_vhdl IS
    PORT ( a, b, c      : IN      BIT;
          f            : OUT     BIT );
END example_vhdl;
```

```
ARCHITECTURE funktion OF example_vhdl IS
BEGIN
    f <= ( c AND b ) OR ( NOT b AND a );
END funktion;
```


Du skal nu bruge simulerings værktøjet til at afprøve funktionen af dit design. Du gør som vist i ”Start af nyt schematic projekt i Quartus II”

Og hvis alt er i orden ender du op med test vektorer som vist nedenfor.



Tegn et kredsløbs diagram over det kredsløb ”vhdl” kildeteksten beskriver.

Udfyld en sandheds tabel for kredsløbet.