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Introduction to the Synchronous Digital Hierarchy (SDH)

The History of Digital Transmission

- ’70s - introduction of PCM into Telecom networks
- 32 PCM streams are Synchronously Multiplexed to 2.048 Mbit/s (E1)
- Multiplexing to higher rates via PDH
- 1985 Bellcore proposes SONET
- 1988 SDH standard introduced.

PDH: Plesiochronous Digital Hierarchy

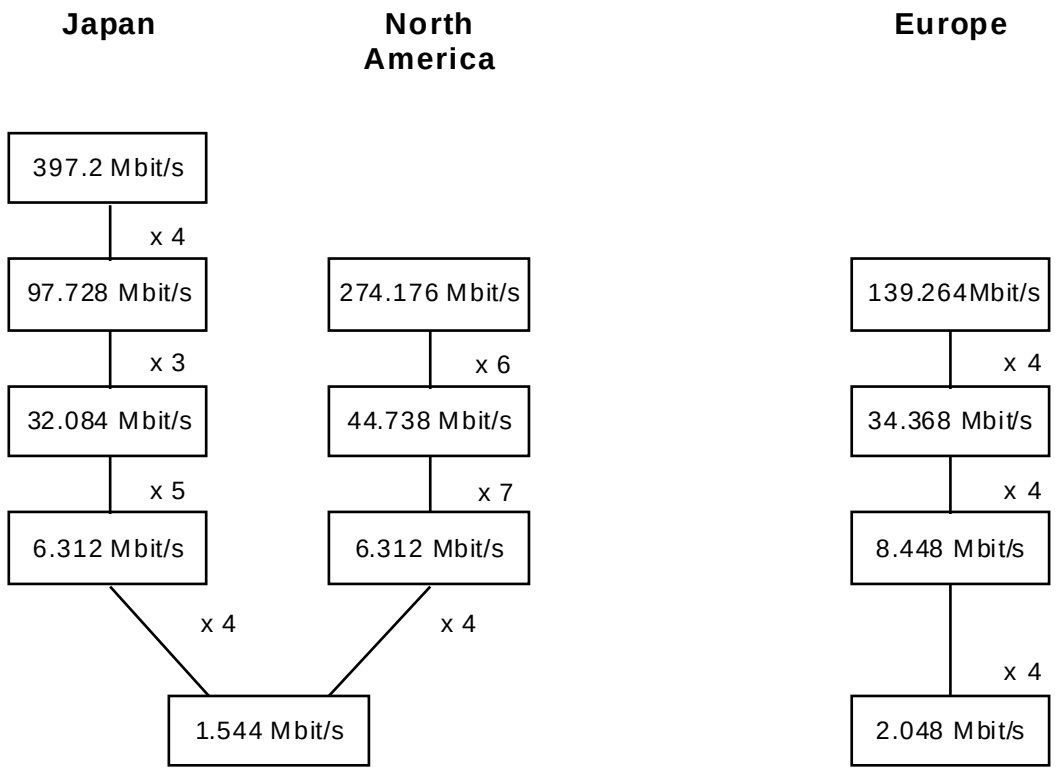
- Multiplex levels:
  - 2.048 Mbit/s
  - 8.448 Mbit/s
  - 34.368 Mbit/s
  - 139.264 Mbit/s
- Uses Positive justification to adapt frequency differences
- Overheads: CRC
- Defects: LOS, LOF, AIS

Plesiochronous Multiplexing

- Before SDH transmission networks were based on the PDH hierarchy.
- Plesiochronous means nearly synchronous.
- 2 Mbit/s service signals are multiplexed to 140 Mbit/s for transmission over optical fiber or radio.
- Multiplexing of 2 Mbit/s to 140 Mbit/s requires two intermediate multiplexing stages of 8 Mbit/s and 34 Mbit/s.
- Multiplexing of 2 Mbit/s to 140 Mbit/s requires multiplex equipment known as 2, 3 and 4 DME.
- Alarm and performance management requires separate equipment in PDH.

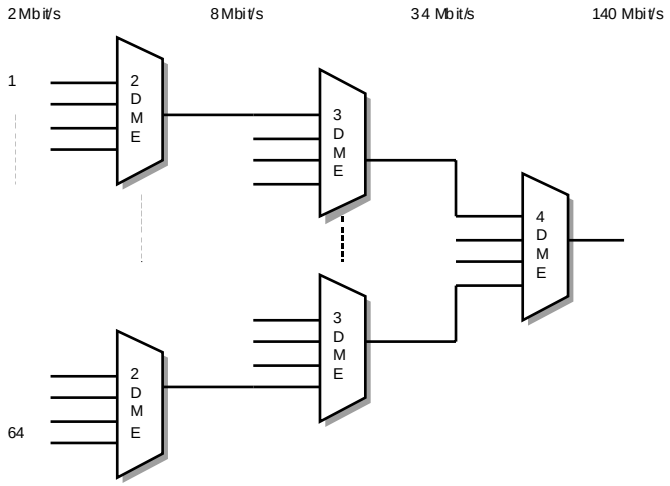
PDH vs. SDH Hierarchy

- PDH transmission rates:
- SDH is designed to unify all transmission rates into a single Mapping hierarchy



PDH Multiplexing

- PDH Multiplexing of 2 Mbit/s to 140 Mbit/s requires 22 PDH multiplexers:
  - 16 x 2DME
  - 4 x 3DME
  - 1 x 4DME
- Also a total of 106 cables required.



PDH Add/Drop

- If a small number of 2 Mbit/s streams passing through a site need to be dropped then in PDH this requires large amount of equipment to multiplex down to 2Mbit/s.

What is SDH?

- The basis of Synchronous Digital Hierarchy (SDH) is synchronous multiplexing - data from multiple tributary sources is byte interleaved.
- In SDH the multiplexed channels are in fixed locations relative to the framing byte.
- Demultiplexing is achieved by gating out the required bytes from the digital stream.
- This allows a single channel to be ‘dropped’ from the data stream without demultiplexing intermediate rates as is required in PDH.

SDH Rates

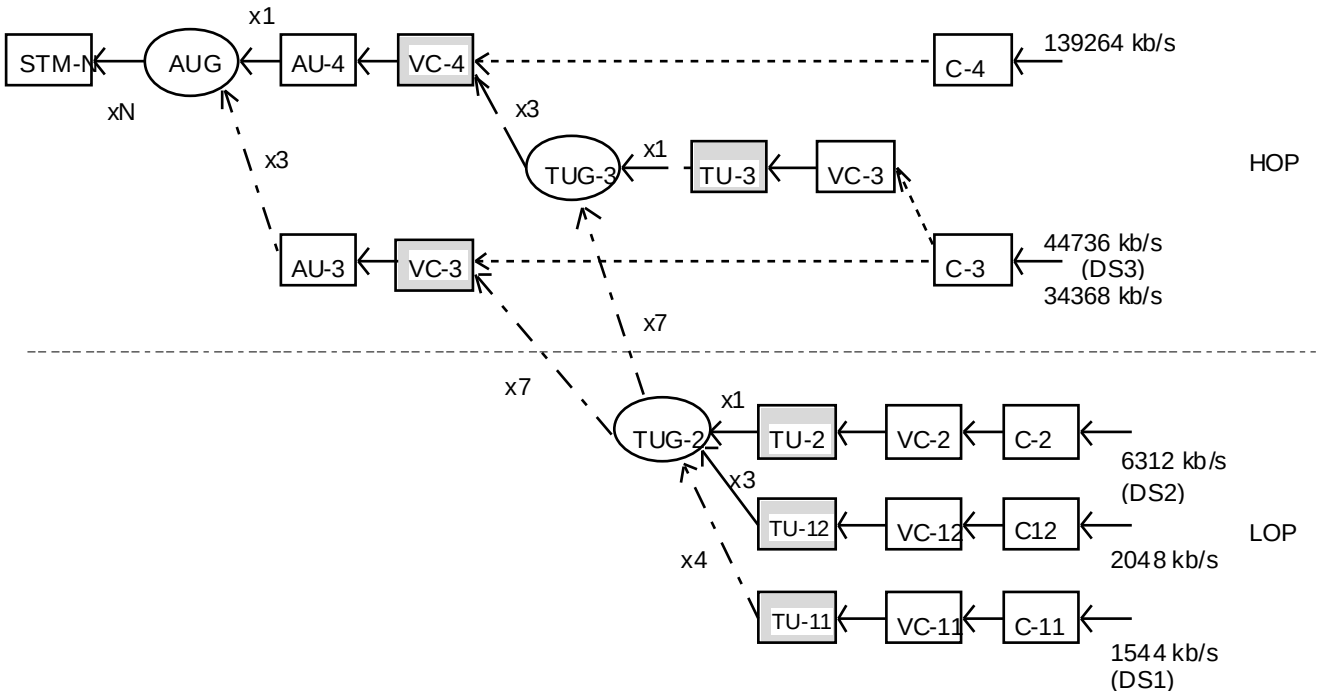
- SDH is a transport hierarchy based on multiples of 155.52 Mbit/s
- The basic unit of SDH is STM-1:

STM-1	=	155.52 Mbit/s
STM-4	=	622.08 Mbit/s
STM-16	=	2588.32 Mbit/s
STM-64	=	9953.28 Mbit/s

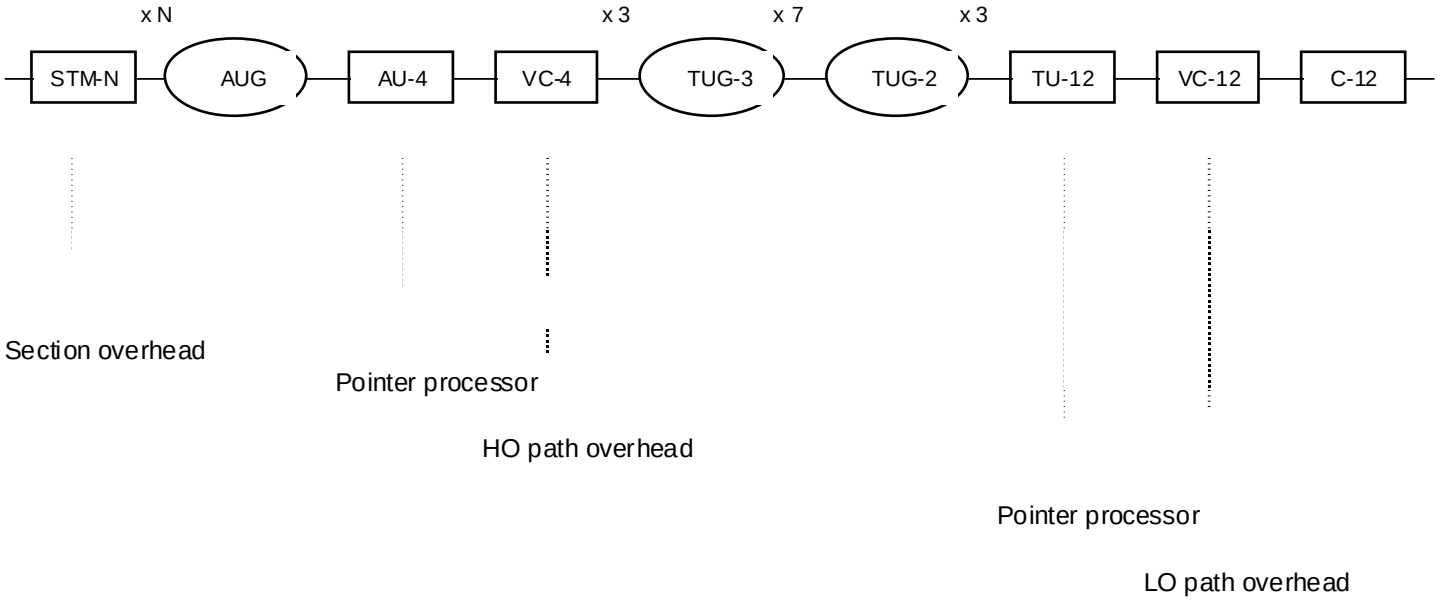
- Each rate is an exact multiple of the lower rate therefore the hierarchy is synchronous.

SDH Hierarchy

- SDH defines a multiplexing hierarchy that allows all existing PDH rates to be transported synchronously.
- The following diagram shows these multiplexing paths:



Example: Multiplex path for the E1

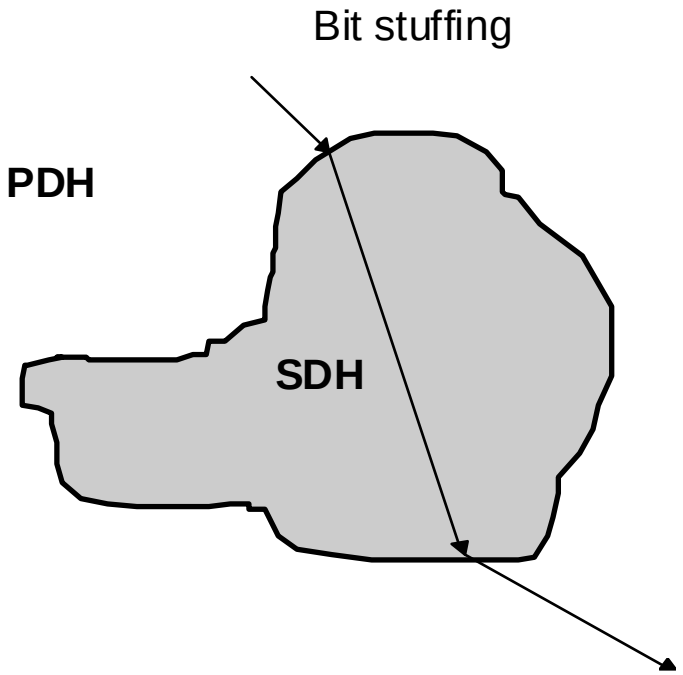


Transport of PDH payloads

- SDH is essentially a transport mechanism for carrying a large number of PDH payloads.
- A mechanism is required to map PDH rates into the STM frame.
- This function is performed by the container (C).
- A PDH channel must be synchronised before it can be mapped into a container.
- The synchroniser adapts the rate of an incoming PDH signal to SDH rate.

SDH and non-synchronous signals

- At the PDH/SDH boundary Bit stuffing is performed when the PDH signal is mapped into its container.

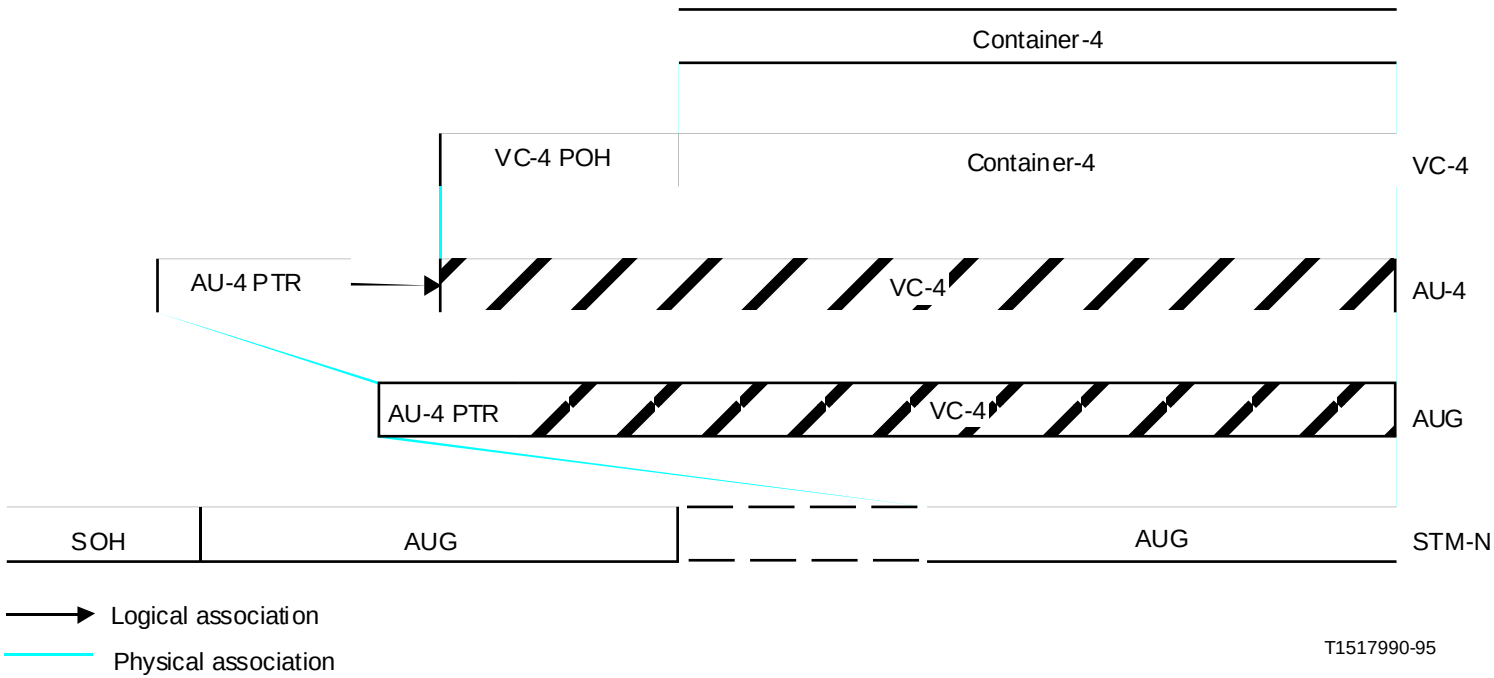


SDH virtual Containers

- Once a container has been created, path overhead byte are added to create a virtual container.
- Path overheads contain alarm, performance and other management information.
- A path through an SDH network exists from the point where a PDH signal is put into a container to where the signal is recovered from the container.
- The path overheads travel with the container over the path.

Mapping Virtual Containers

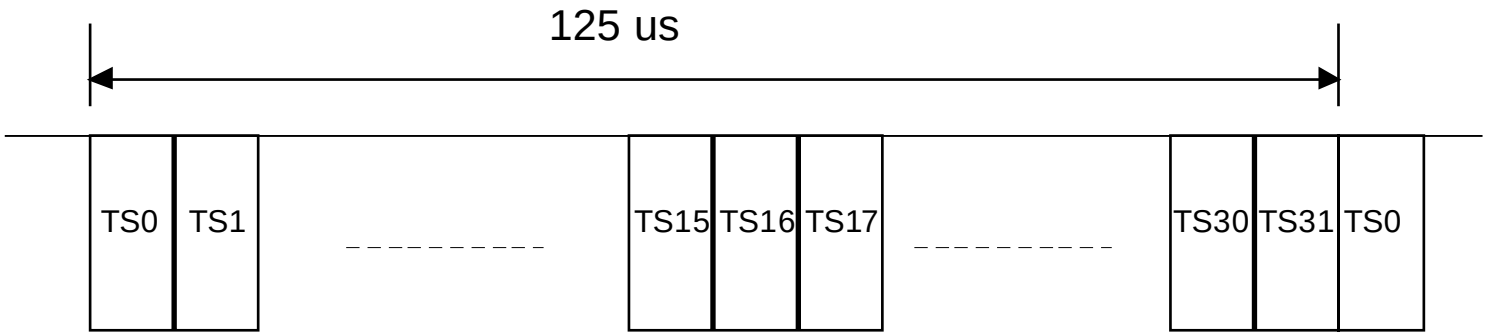
- C-4 container being mapped into an STM frame via a VC-4 virtual container



NOTE – Unshaded areas are phase aligned. Phase alignment between the unshaded and shaded areas is defined by the pointer (PTR) and is indicated by the arrow.

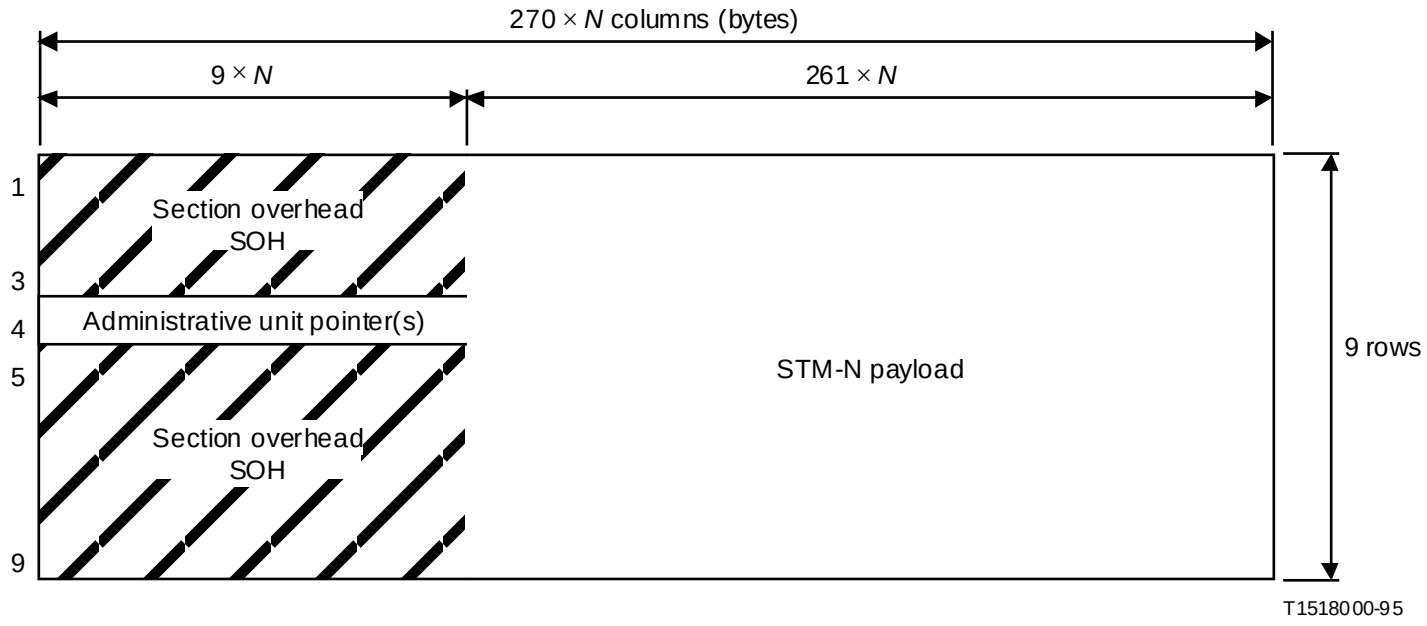
2 Mbit/s PCM30 frame structure

- The SDH frame rate is inherited from PCM.
- As with PCM, the SDH has 8 bits per time slot.
- As with PCM, the SDH frame rate in 125 us per frame.
- The following diagram shows the PCM30 frame:



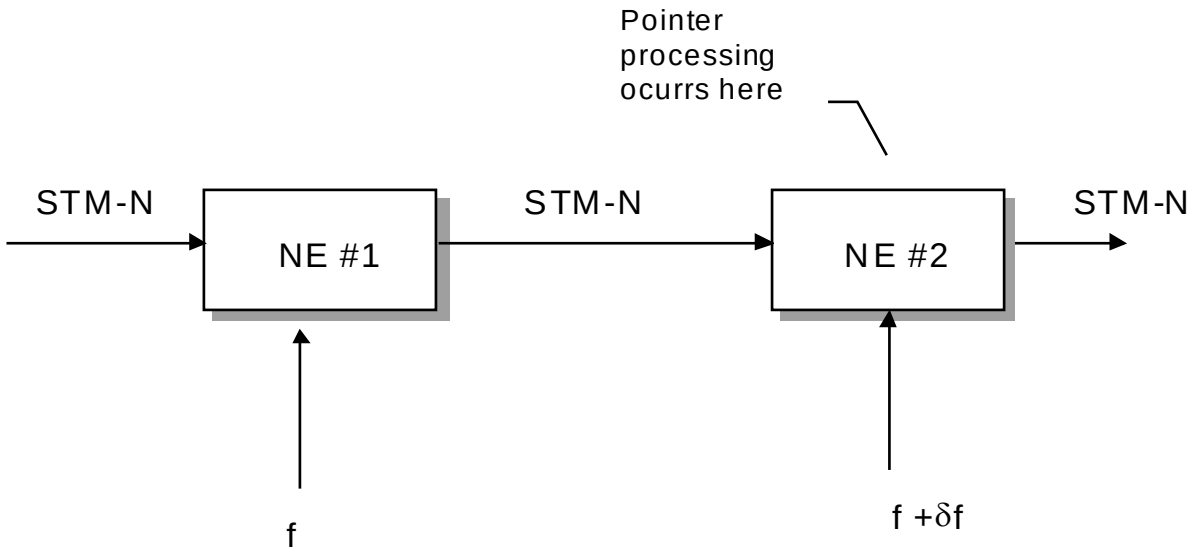
Basic SDH frame structure

- STM-N frame structure is shown in the Figure below. The three main areas of the STM-N frame are indicated:
  - SOH;
  - Administrative Unit pointer(s);
  - Information payload.



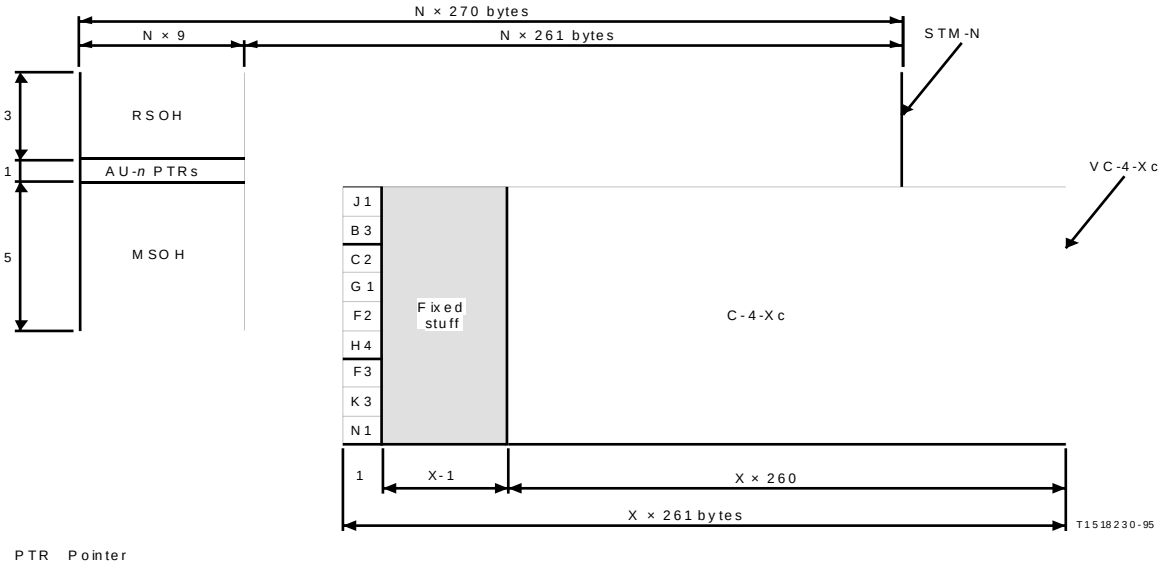
Different clock rates in SDH

- SDH will still work if there are two different clocks in the network and the network becomes asynchronous.
- Pointers are used adjust for the new frequency.



Administrative Units in the STM-N

- The VC-4 is mapped into an STM frame via the administrative group (AU).
- The VC-4 associated with each AU-4 does not have a fixed phase with respect to the STM-N frame.
- The location of the first byte of the VC-n is indicated by the AU-n pointer.

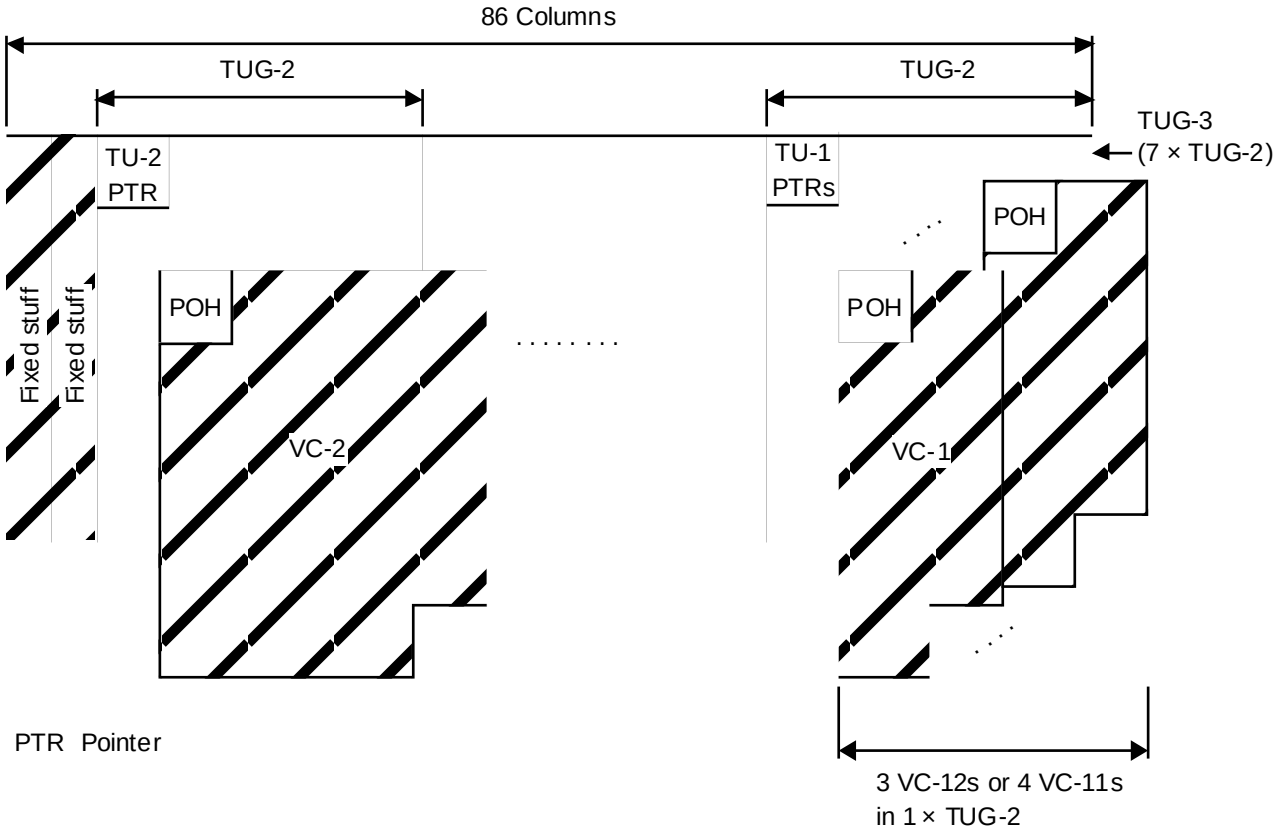


PTR Pointer

Tributary Units in a VC-4

- The VC-4 can carry a container -4 (C-4). The C4 carries a 140 Mbit/s PDH signal.
- The VC-4 forms what is known as an high order path.
- If lower speed PDH signals need to be transported these are mapped into a tributary unit (TU).
- The TUs are then multiplexed into a VC-4.
- The VC-n associated with each TU-n does not have a fixed phase relationship with respect to the start of the VC-4.
- The TU-n pointer is in a fixed location in the VC-4 and the location of the first byte of the VC-n is indicated by the TU-n pointer.

Tributary Units in a VC-4



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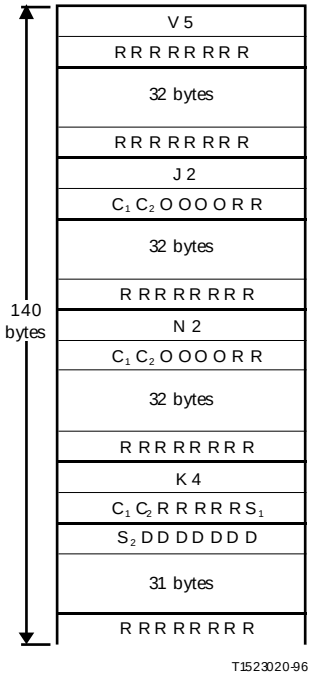
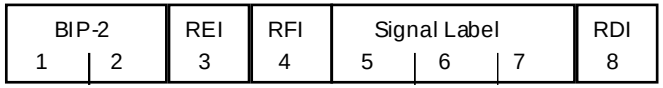
Tributary units



D Data bit
R Fixed stuff bit
O Overhead bit
S Justification opportunity bit
C Justification control bit

- 2 Mbit/s are mapped asynchronously into a VC-12.
- VC-12s are distributed over four frames known as a VC multiframe.
- The figure shows this over a period of 500 µs.

- V5 byte:



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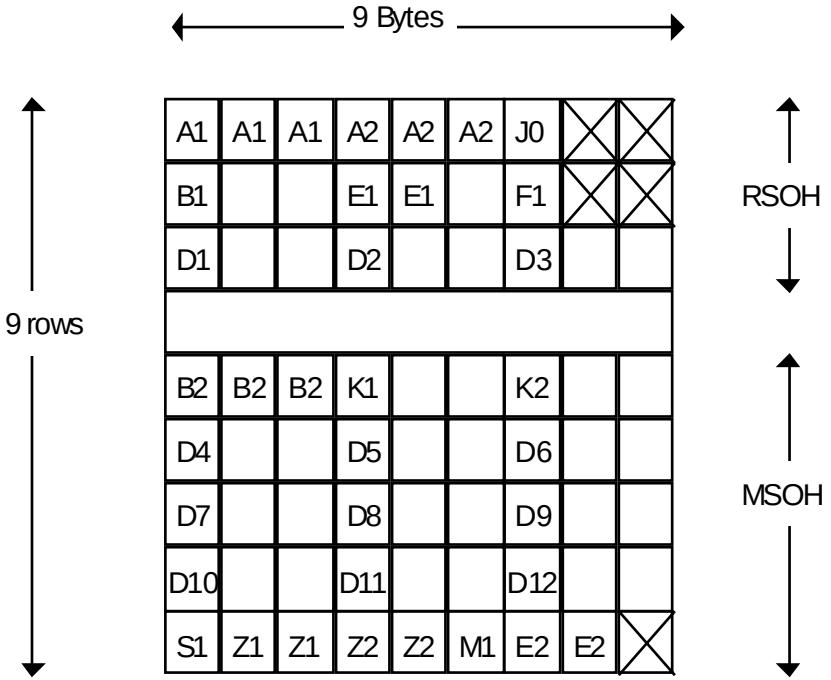
STM Section Overheads

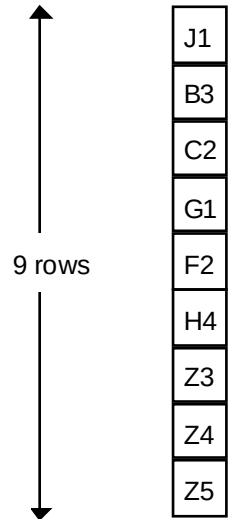
- Nine rows of nine bytes at the front of the SDH frame form the section overhead.
- The first three rows are the regenerator section overhead.
- The last six rows are the multiplex section overhead.



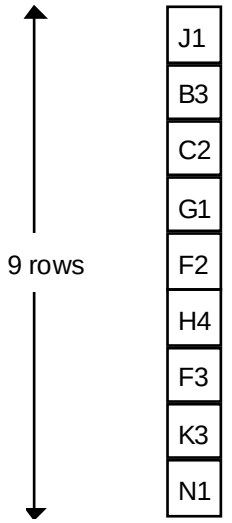
VC-4 path overheads

- The first column of the VC-4 is the VC-4 path overhead.
- The overheads have been modified in the latest release of G.707

Old VC-4 POH

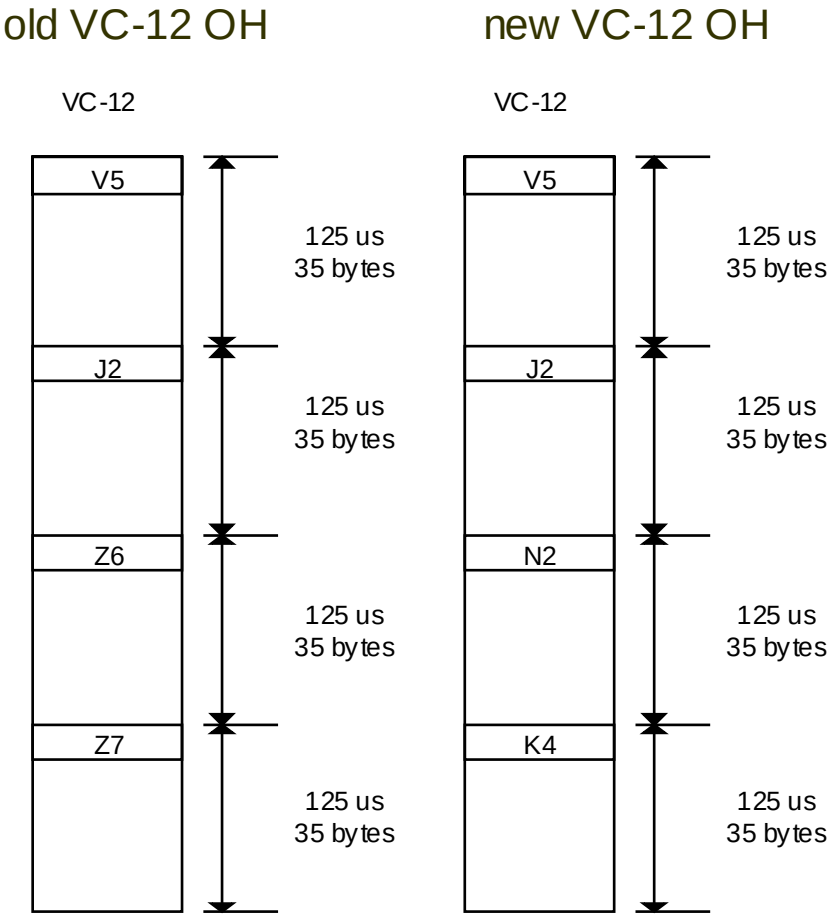


new VC-4 POH



VC-12 overhead

- The first byte of the VC-12 is the VC-12 path overhead.
- The VC-12 frame is spread over four frames to form a VC-12 multiframe.
- Each of the four frames in the multiframe contains an overhead byte.
- The overheads have been modified in the latest release of G.707



V5 Byte

- The bits in the V5 byte are allocated as follows:

BIP-2		REI	RFI	Signal Label			RDI
1	2	3	4	5	6	7	8

Framing bytes (A1 & A2)

- The framing byte locate the beginning of the STM frame

Byte	comments
A1	First framing byte A1:11110110
A2	Second framing byte A2:00101000

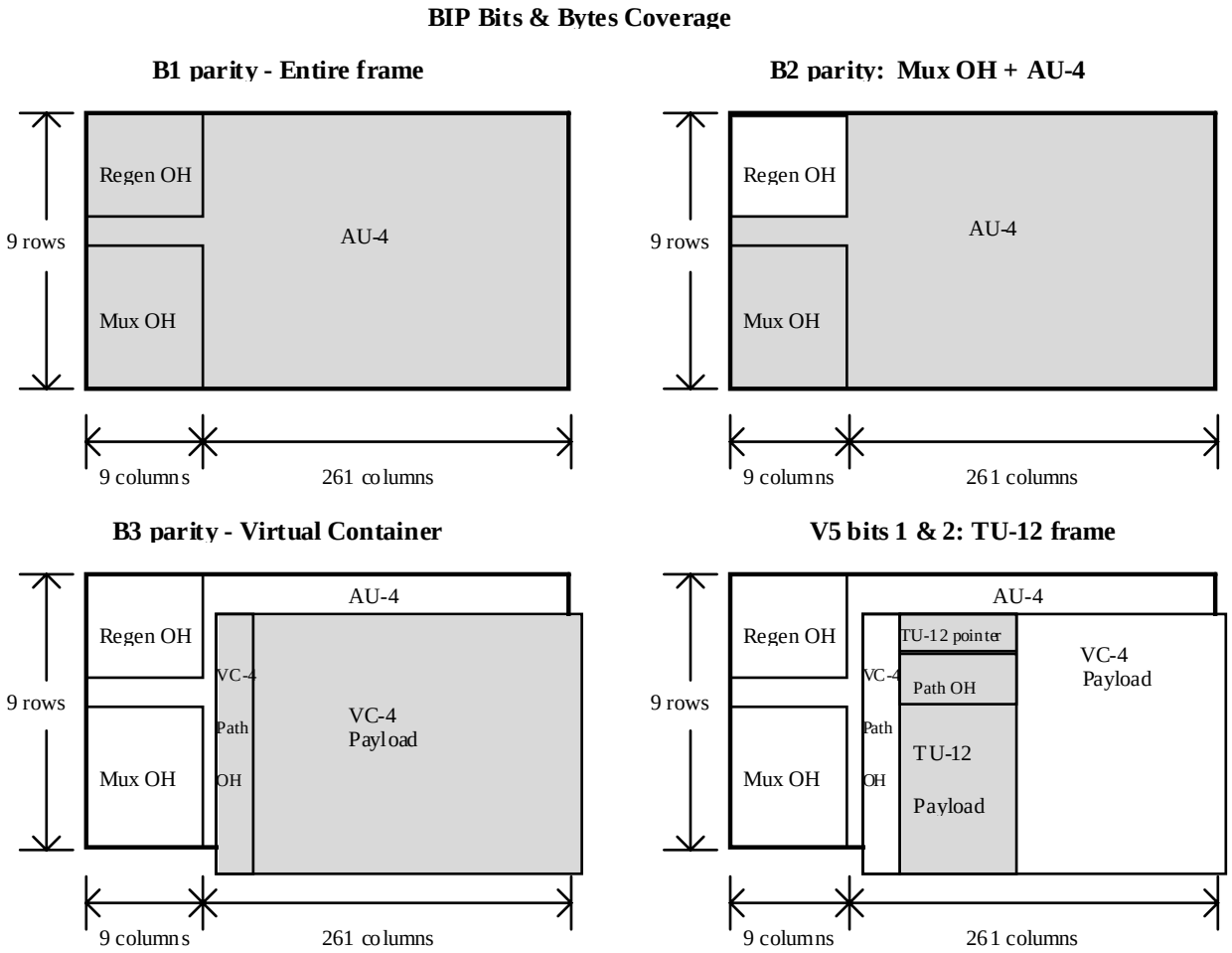
Synchronisation status marker byte (S1).

- The synchronisation status marker byte contains information about the quality of the embedded timing

Byte	comments
S1	Synchronistion status marker byte **S1 Byte: bit 5 -8** 0000 Quality unknown 0010 Traceable to PRC G.811 0100 Traceable to Transit G.812 1000 Traceable to Local G.812 1011 Derived from SETS 1111 Don't use for Synchronisation. Other bytes are reserved.

Bit interleaved parity (B1, B2, B3)

- The BIP is calculated over the previous frame/multiframe



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Bit interleaved parity (B1, B2, B3)

Byte	comments
B1	Bit interleaved parity - 8 bits for entire previous frame before scrambling.
B2 #1,2,3	Three bytes of a 24 bit multiplex section bit interleaved parity - Calculated over the previous STM-1 frame excluding the first three rows of the SOH before scrambling.
B3	Bit interleaved parity - 8 bits for entire previous frame before scrambling. The BIP is calculated over the previous VC-4.
V5	VC-12 path bit interleaved parity - 2 bits for previous frame The BIP is calculated over the previous VC-12 frame including VC-12 path overheads but excludes V1, V2, V3.

Orderwire (E1 & E2)

- The E byte carry the orderwire channels.
- The relief byte is used for ring protection

  - E1 – Regenerator section orderwire
  - E2 – Multiplex section orderwire

DCC channels (D1 to D3 and D4 to D12)

- The DCC channels are used Element Management Software to pass management information between sites.

Byte	comments
D1 to D3	Regenerator section data communications channel (DCC) The D1 to D3 bytes are a 192 kbit/s DCC channel.
D4 to D12	Multiplex section data communications channel The D4 to D12 bytes are a 576 kbit/s DCC channel.

User channels (F1, F2, F3 & N2)

- The user channels appear at a front panel connector for use by the network operator.

Byte	comments
F1 User channel	64 kbit/s user channel. The FLX150/600 supports either G.703 co-directional or contradirectional interface. This user channel can be passed through at a regenerator.
F2	VC-4 path user channel
Z3 (F3) **Z6 (N2)**	VC-4 path user channel Network operator byte -

Section/Path trace bytes (J0, J1, J2)

- The section/path trace supports a string assigned to a path, this verifies continued connection to the intended transmitter

Byte	comments
J0	Regenerator section trace use is not defined in ITU-T. Trace value can be entered for section id between national boundaries.
J1	ITU-T: High order path access point identifier.
J2	Path trace byte

Remote error indication

- MS REI (M1) Indicates the count of the interleaved bit blocks (1 to N) that have detected an error.

Byte	comments
M1	Multiplex section remote error indication (MS REI)

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High order path management

- Signal label (C2)

Byte	comments
C2	Signal label: This byte indicates the composition of the VC-4 .

- Path Status

Byte	comments
G1	Path status byte. This byte is sent from the receiver back to the originator.

- Multiframe Pointer

Byte	comments
H4	VC-4 multiframe pointer. Indicates the multiframe position indicator for the VC-12

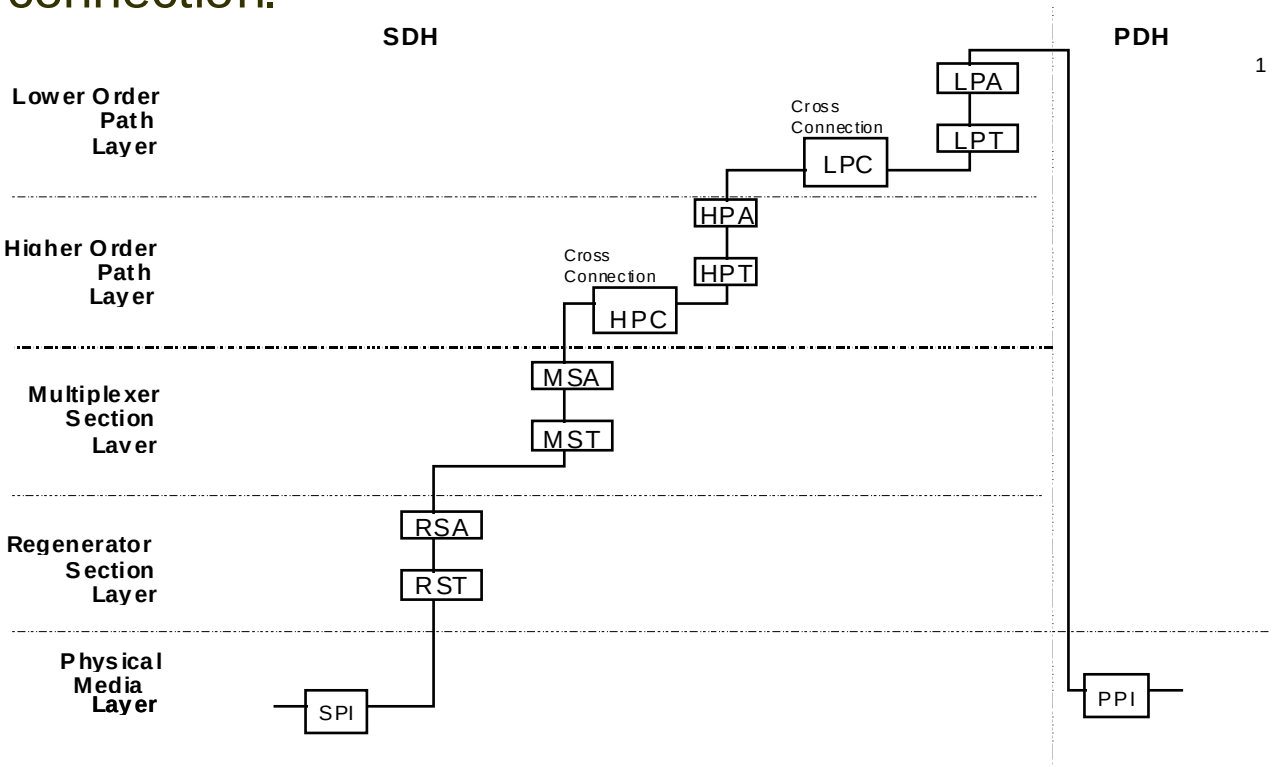
Low order path management

- The VC-12 path overhead signals are held in the V5 byte.

Byte	Comments
V5 bit 3	Remote error indication (REI): set to one if one or more error is detected at receiver in the BIP-2. Standard implementation on FLX and FLM
V5 bit 4	Remote failure indication (RFI). Set to one if a failure is declared .
V5 bit 5-7 V5 bit 8	VC-12 signal label. VC-12 path remote defect indication (RDI) Set to 1 if an AIS or a signal failure condition is received.

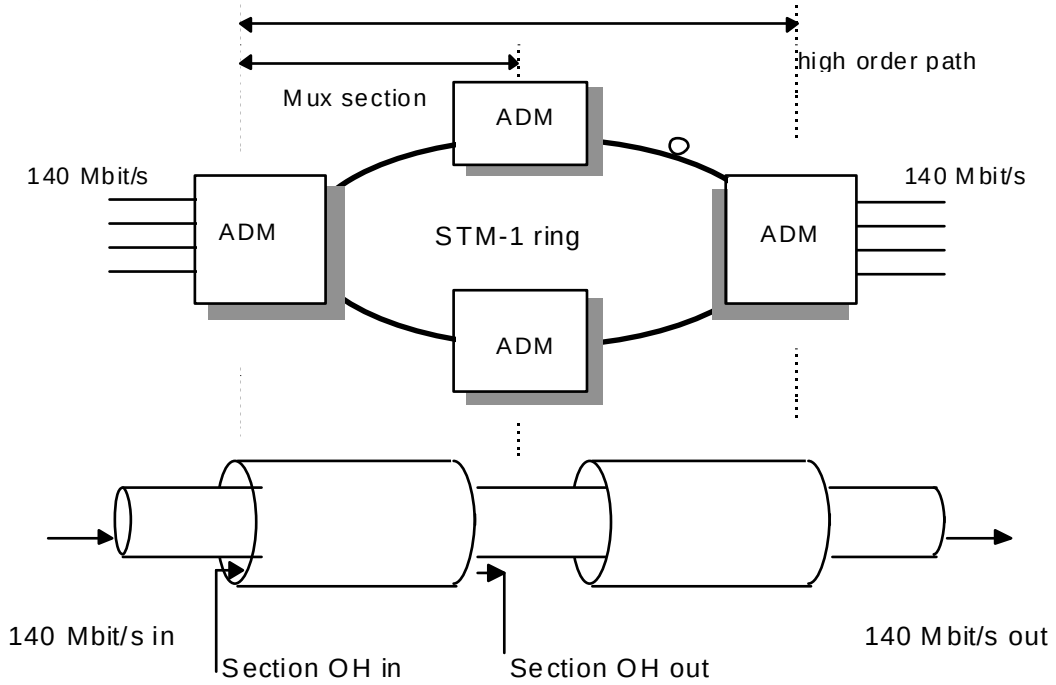
SDH layers

- The following diagram shows 2Mbit/s multiplexed to STM-1.
- The transmission path passes through five layers in this connection.

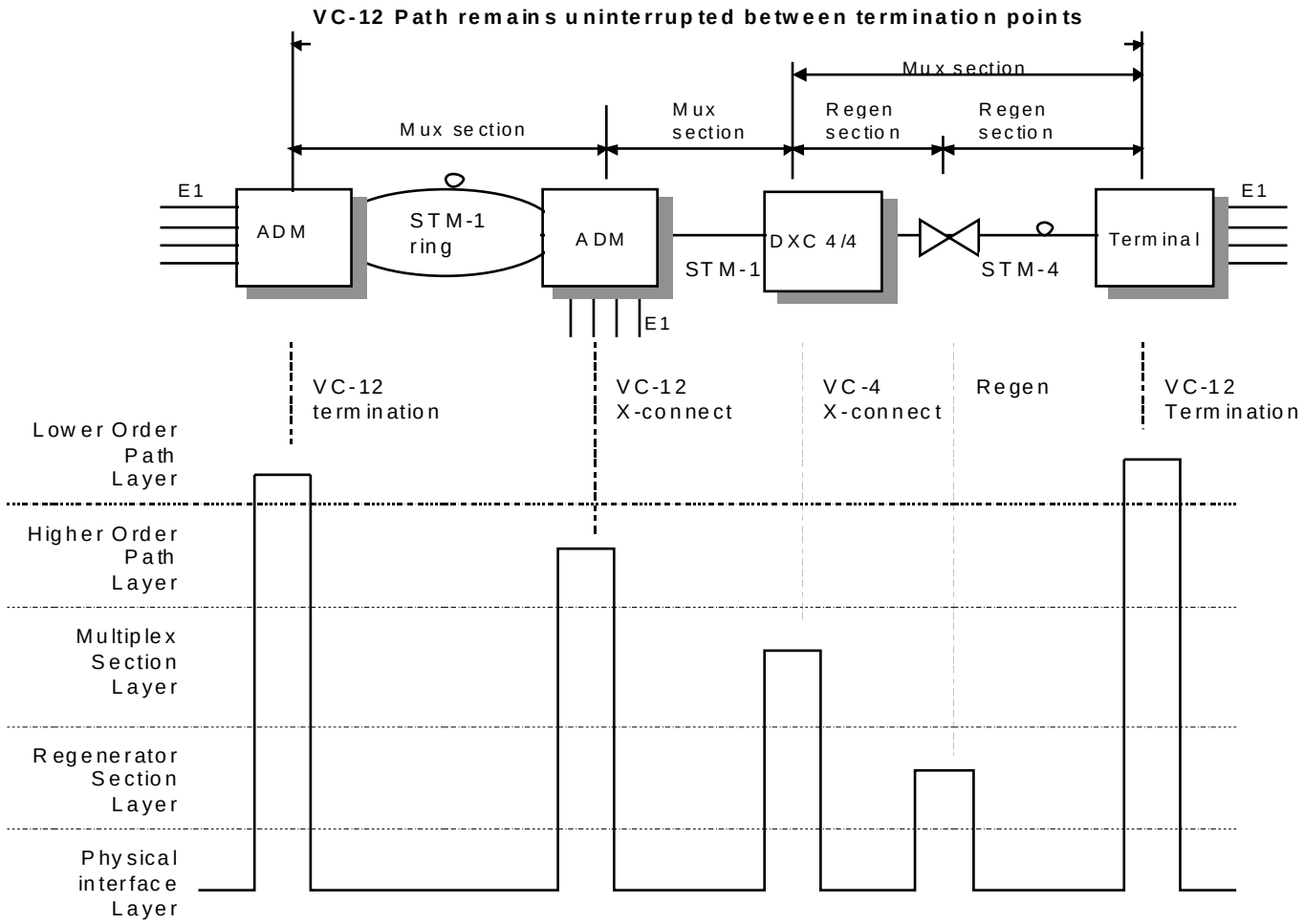


Termination points

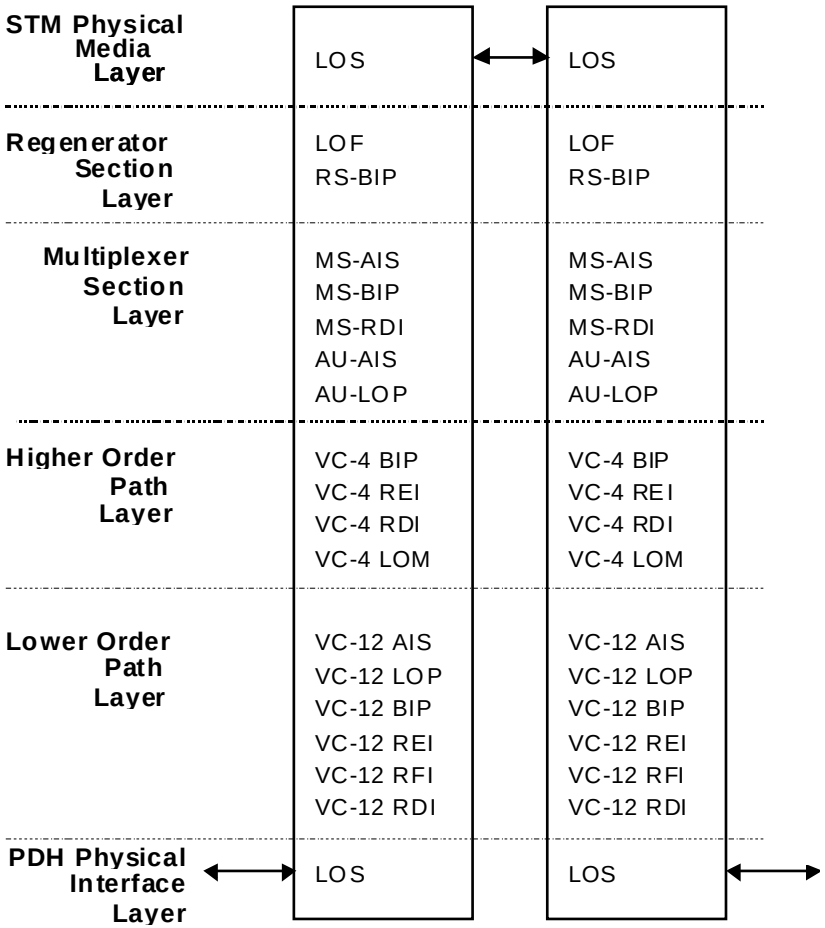
- Within a layer each path ends at a ‘termination point’
- A path in SDH can be visualised as a pipe, In the diagram the 140Mbit/s path passes unaltered through the multiplex section0



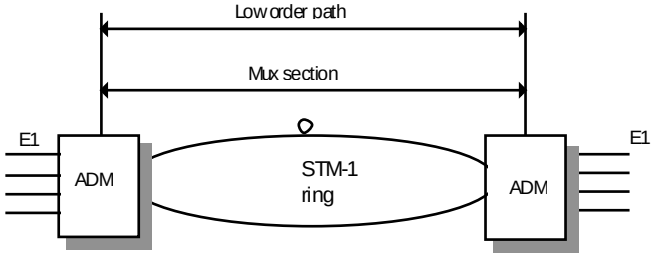
Layers - Example



Alarms and layers

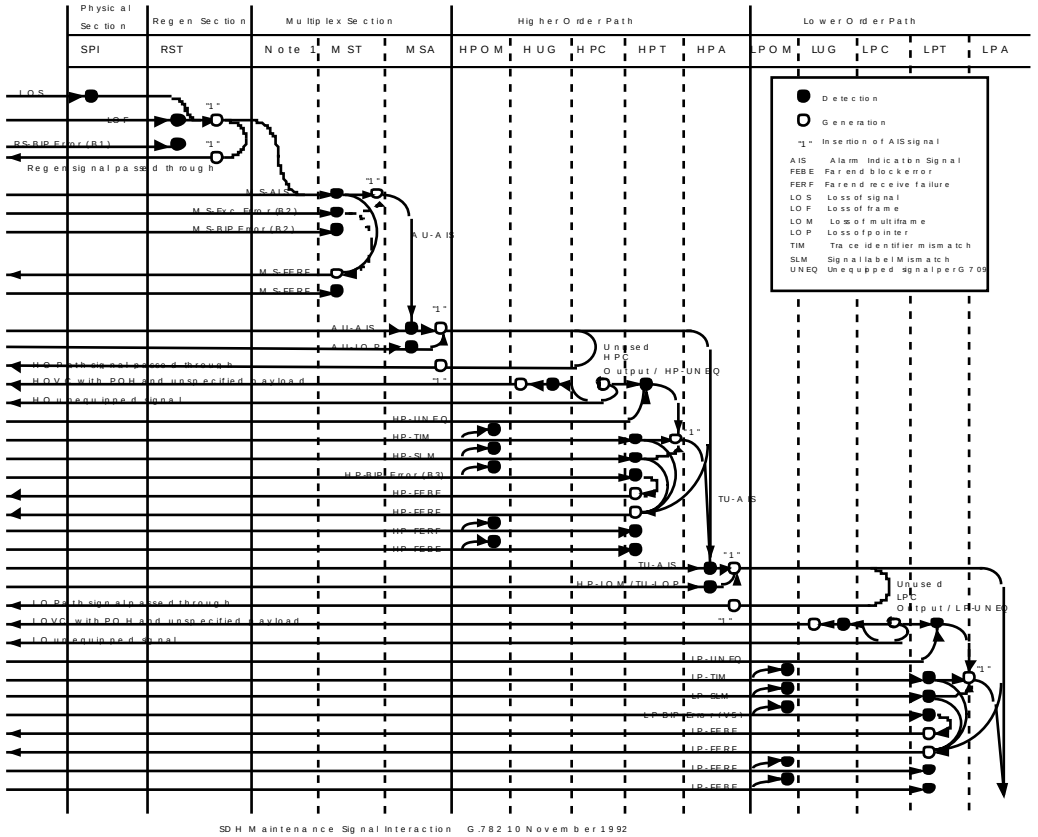


- Each defect indication is associated with a layer



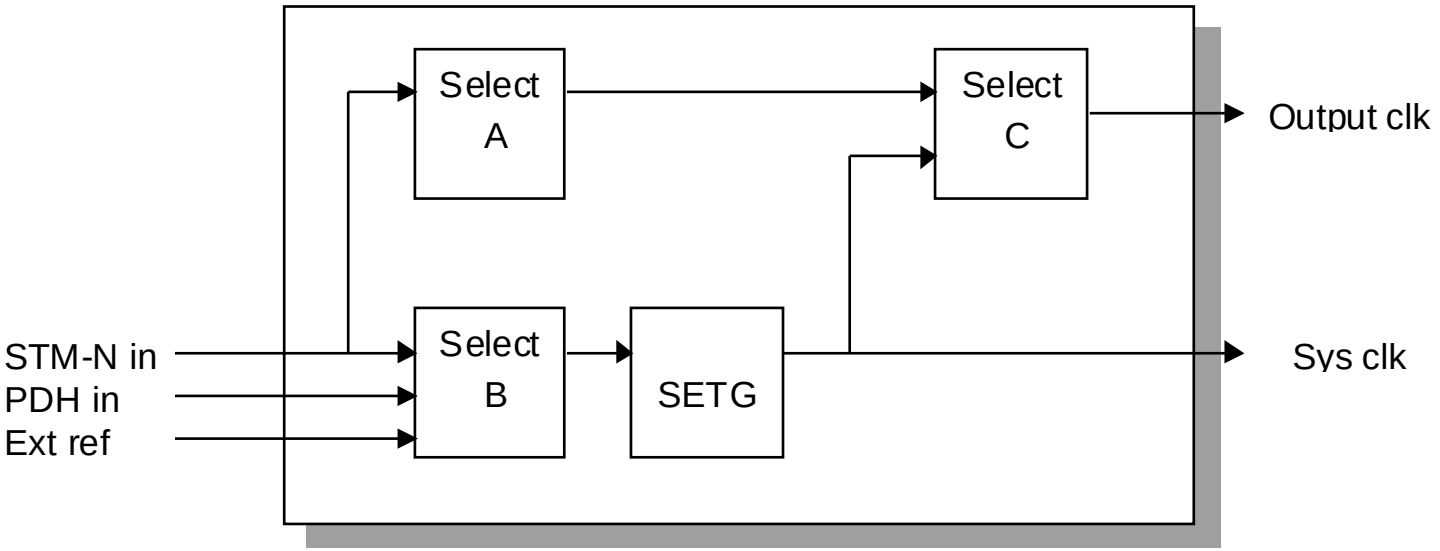
Signalling interactions

- Each signal has a consequent action. These are described in the G.782 diagram



SETS: Synchronous Equipment Timing Source

- The SETS function controls the selection of the timing source to be used as a reference in the SDH equipment
- The SETG function is a DPLL function that smoothes the clock and provides holdover on loss of clock.



Sync distribution in the SDH network

- SDH can be used as a timing transport in a telecommunications network.
- In this case a SETG (DPLL) is in the clock path at each network element (NE)
- The PRC is the network providers primary reference clock
- The G.812 clock is the network providers exchange clock.